An integrated electron spin resonance (ESR) circuit chip includes a chip substrate, a transmitter circuit, and a receiver circuit. The transmitter circuit and receiver circuit are disposed on the chip substrate. The transmitter circuit includes an oscillator circuit configured to generate an oscillating output signal and a power amplifier (PA) circuit configured to generate an amplified oscillating output signal based on the oscillating output signal. The receiver circuit receives an ESR signal from an ESR probe. The receiver circuit includes a receiver amplifier circuit configured to generate an amplified ESR signal based on the received ESR signal, a mixer circuit configured to receive the amplified ESR signal and to down-convert the amplified ESR signal to a baseband signal, and a baseband amplifier circuit configured to generate an amplified baseband signal based on the baseband signal.
(58) Field of Classification Search
CPC .................. G01R 33/3621; G01R 33/323; G01R 33/3407; G01N 24/10; A61B 5/055; G01S 7/023; G01V 3/32; H03D 2200/009; H03D 7/1491; H04B 17/0085; H04B 17/14; H04B 1/525; H04L 7/0054
See application file for complete search history.

(56) References Cited
U.S. PATENT DOCUMENTS
2013/0093424 A1* 4/2013 Blank ....................... G01R 33/60 324/316
2013/0257431 A1* 10/2013 Tseitlin ..................... G01R 33/60 324/316

OTHER PUBLICATIONS

* cited by examiner
FIG. 3

Inverting Comparator

Set

Pulse

Set'
FIG. 9A

- 22-26GHz VCO
- VCO Buffer
- RF Buffer
- PA
- To Resonator
- From Pulse Generator
- LO Buffer
- To Mixer LO
- 901
- 903
- 905
- 907
- 909
- 911
FIG. 9C
DC Magnet

DC Magnetic Field
$(B_0)$

RF Magnetic Field
$(B_1)$

Sample

1213

On-Chip Resonator

1200a

Silicon Chip

1200b

Excitation

Detection

FIG. 12A

FIG. 12B
FIG. 13A
Digital Pulse Output
Clock (Set) Signal

FIG. 13B
Digital Pulse Output
Clock (Set) Signal
FIG. 14A

FIG. 14B
FIG. 16
FIG. 17A

Digital Pulse Output

Clock (Set) Signal

FIG. 17B
### SoC Specifications

<table>
<thead>
<tr>
<th>Process</th>
<th>IBM 8HP 0.13µm SiGe BiCMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die specifications</td>
<td>2.5mm x 1.5mm, 59 pins (8 test)</td>
</tr>
<tr>
<td>Power consumption</td>
<td>425mW</td>
</tr>
<tr>
<td>Operating Voltage</td>
<td>2.0V and 1.5V (analog), 1.2V (digital)</td>
</tr>
</tbody>
</table>

#### Transmitter

| VCO frequency range | 770MHz – 970MHz |
| PA power gain | 15dB |
| RF pulse width (in pulse mode) | 20ns – 400ns |

#### Receiver (designed values)

| LNA Power gain | 40dB |
| LNA Noise figure | 3.7dB |
| LNA 1dB compression point | -15dBm (Output referred) |

#### Programmable pulse generator

| Pulse width | 20ns to 400ns |
| Pulse width resolution | 0.5ns |

---

**Figure S3: SoC specifications.**

---

**FIG. 18A**

---

### SoC Specifications

<table>
<thead>
<tr>
<th>Process</th>
<th>IBM 8HP 0.13µm SiGe BiCMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die specifications</td>
<td>1mm x 2mm, 54 pins (47 I/O, 7 test)</td>
</tr>
<tr>
<td>Power consumption</td>
<td>385mW</td>
</tr>
<tr>
<td>Operating Voltage</td>
<td>2.0V and 1.5V (analog), 1.2V (digital)</td>
</tr>
</tbody>
</table>

#### Transmitter

| Operation frequency | 22-26GHz |
| Pulse Frequency | 1-10MHz |
| Pulse Width | 0.5ns-500ns |
| Pulse Resolution | 400ps |
| Transmitter Gain | 936A/W (excitation current/VCO output power) |

#### Receiver

| Operation Frequency | 22-26GHz |
| LNA Voltage Gain | 61dB |
| Receiver Gain | 244W/A (baseband output power/detection current) |

---

**FIG. 18B**
FIG. 19A

FIG. 19B
INTERGATED ELECTRON SPIN RESONANCE SPECTROMETER

CROSS-REFERENCE TO RELATED APPLICATIONS

This Application claims priority, pursuant to 35 U.S.C. §119(e), to U.S. Provisional Application No. 61/707,441, the contents of which is incorporated by reference herein in its entirety.

BACKGROUND

Electron spin resonance (ESR), also equivalently referred to herein as electron paramagnetic resonance (EPR), is a spectroscopic and imaging technique that is capable of providing quantitative information regarding the presence and concentration of a variety of magnetic species within a sample under test, e.g., a biological tissue sample. The valence electron(s) of a magnetic species possess unpaired angular momentum and thus, have net magnetic moments that tend to align along an externally applied magnetic field. This alignment process is known as magnetization. ESR is a measurement technique that relies on the external manipulation of the direction of this electron magnetization, also referred to as a net electronic magnetic moment. In a typical ESR experiment, a polarizing magnetic field $B_0$ is applied to a sample to align the magnetic moments of the electrons along the direction of the magnetic field $B_0$. Then, an oscillating magnetic field $B_1$, often referred to as the transverse magnetic field, is applied along a direction that is perpendicular to the polarizing field $B_0$. Usually the oscillating field $B_1$ is generated using a microwave resonator (a coil or a transmission line) and is designed to excite the unpaired electrons by driving transitions between the different angular momentum states of the unpaired electron(s).

Currently there are two major techniques used to perform ESR spectroscopy. The first is a continuous wave (CW), frequency domain method and the second is a pulse-based, time domain technique. A CW spectrometer utilizes a continuous, narrow-band signal to create $B_1$, and thus, energize unpaired electrons in the presence of the external DC magnetic field $B_0$. In CW spectroscopy, an absorption spectrum of the sample is obtained by either sweeping the frequency of $B_1$ while $B_0$ is kept constant or by sweeping $B_0$ while the frequency of $B_1$ is kept constant. CW spectroscopy has been traditionally used for ESR because it is simpler in terms of circuitry and is able to detect samples even with very fast relaxation times (tens of nanoseconds). However, direct measurement of certain spin relaxation parameters, such as the longitudinal relaxation time, also referred to as the spin-lattice relaxation time ($T_1$) and/or the transverse relaxation time, also referred to as the spin-spin relaxation time ($T_2$) is feasible using time domain or pulse techniques. In pulse ESR, instead of sweeping a continuous signal, $B_1$ is pulsed in a precisely designed pulse sequence to manipulate the direction of the spins of the unpaired electrons. The subsequent time-domain ESR signal emitted from the electrons as they relax back to their equilibrium state is then recorded by a receiver resonator. In pulsed ESR, wideband spectral information relating to the ESR samples may be reproduced using Fourier transform techniques applied to the ESR signal.

Presently, ESR imaging and spectroscopy are conducted using systems that employ a large number of discrete radiofrequency (RF) or microwave components. For example, current systems employ discrete RF sources, pulse generators, power amplifiers, lock-in amplifiers, resonators, mixers, analog-to-digital converters, connecting cables, etc. However, as the instrument sizes exceed the characteristic wavelengths corresponding to the ESR experiment frequency (typically less than 1 meter, corresponding to a frequency of 300 MHz) the spectrometer/imager becomes sensitive to radiative effects and noise from the ambient RF radiation. This results in noisy and/or unstable data. Furthermore, the weight of the magnets and the RF components is typically hundreds of kilograms thereby prohibiting the portability of currently existing ESR spectrometers/imagers. Furthermore, the cost of building an ESR imager from discrete components can be prohibitively high. Finally large, discrete ESR imagers also have slow response times. This becomes a key limitation for time-domain imaging/spectroscopy, where the response time of the imager determines the shortest relaxation time that can be detected using time-domain ESR. Current in-vivo ESR imagers have response times that are limited to 1 microsecond or greater.

SUMMARY

This summary is provided to introduce a selection of concepts that are further described below in the detailed description. This summary is not intended to identify key or essential features of the claimed subject matter, nor is it intended to be used as an aid in limiting the scope of the claimed subject matter.

In general, in one aspect, one or more embodiments are directed to an integrated electron paramagnetic resonance (ESR) circuit chip that includes a chip substrate, a transmitter circuit, and a receiver circuit. The transmitter circuit and receiver circuit are disposed on the chip substrate. The transmitter circuit includes an oscillator circuit configured to generate an oscillating output signal and a power amplifier (PA) circuit configured to generate an amplified oscillating output signal based on the oscillating output signal. The receiver circuit receives an ESR signal from an ESR probe. The receiver circuit includes a receiver amplifier circuit configured to generate an amplified ESR signal based on the received ESR signal, a mixer circuit configured to receive the amplified ESR signal, a PA circuit configured to generate an amplified oscillating output signal based on the oscillating output signal, and a baseband amplifier circuit configured to generate an amplified baseband signal based on the baseband signal.

In general, in one aspect, one or more embodiments are directed to an integrated ESR spectrometer. The integrated ESR spectrometer includes an ESR probe and an integrated ESR transceiver chip. The ESR probe includes a magnet configured to generate a bias magnetic field in a bias field direction and a resonator configured to generate an oscillating magnetic field having a direction that is substantially perpendicular to the bias field direction. The integrated ESR transceiver chip includes a chip substrate, a transmitter circuit, and a receiver circuit. The transmitter circuit and receiver circuit are disposed on the chip substrate. The transmitter circuit includes an oscillator circuit configured to generate an oscillating output signal and a PA circuit configured to generate an amplified oscillating output signal, based on the oscillating output signal. The receiver circuit is configured to receive an ESR signal from the resonator. The receiver circuit includes a receiver amplifier circuit configured to generate an amplified ESR signal based on the received ESR signal, a PA circuit configured to receive the amplified ESR signal and down-converts the amplified ESR signal to a baseband signal, and a baseband
amplifier circuit configured to generate an amplified baseband signal based on the baseband signal.

Other aspects of the invention will be apparent from the following description and the appended claims.

BRIEF DESCRIPTION OF DRAWINGS

FIGS. 1A-1B show an integrated electron spin resonance (ESR) spectrometer in accordance with one or more embodiments of the invention.

FIG. 2 show an integrated electron spin resonance (ESR) spectrometer in accordance with one or more embodiments of the invention.

FIG. 3 show an integrated programmable pulse generator circuit in accordance with one or more embodiments of the invention.

FIGS. 4A-4C show an integrated transmitter circuit in accordance with one or more embodiments of the invention.

FIGS. 5A-5B show an integrated receiver circuit in accordance with one or more embodiments of the invention.

FIG. 6A shows a micrograph of an integrated transceiver circuit in accordance with one or more embodiments of the invention.

FIG. 6B-6H show the metal layers of a multi-layer chip layout in accordance with one or more embodiments of the invention. FIGS. 6B, 6C, 6D, 6E, 6F, 6G, and 6H correspond to layers M7 or AM (aluminum, top layer), M6 or LY (aluminum), M5 or MQ (copper), M4 (copper), M3 (copper), M2 (copper), and M1 (copper, bottom layer).

FIG. 7A-7C show an integrated ESR spectrometer in accordance with one or more embodiments of the invention.

FIG. 8 shows an active leakage cancellation circuit in accordance with one or more embodiments of the invention.

FIGS. 9A-9D shows an integrated transmissive circuit in accordance with one or more embodiments of the invention.

FIGS. 10A-10C show an integrated receiver circuit in accordance with one or more embodiments of the invention.

FIG. 11A is a micrograph of an integrated transceiver circuit in accordance with one or more embodiments of the invention.

FIGS. 11B-11H show the metal layers of a multi-layer chip layout in accordance with one or more embodiments of the invention. FIGS. 6B, 6C, 6D, 6E, 6F, 6G, and 6H correspond to layers M7 or AM (aluminum, top layer), M6 or LY (aluminum), M5 or MQ (copper), M4 (copper), M3 (copper), M2 (copper), and M1 (copper, bottom layer).

FIGS. 12A-12B show an integrated ESR spectrometer in accordance with one or more embodiments of the invention.

FIGS. 13A-13B show test data for an integrated programmable pulse generator circuit in accordance with one or more embodiments of the invention.

FIGS. 14A-14B show test data for an integrated voltage controlled oscillator circuit in accordance with one or more embodiments of the invention.

FIG. 15 shows test data for an integrated transceiver circuit in accordance with one or more embodiments of the invention.

FIG. 16 shows test data for an integrated transceiver circuit in accordance with one or more embodiments of the invention.

FIG. 17A-17B shows test data for an integrated transceiver circuit in accordance with one or more embodiments of the invention.

FIG. 18A-18B shows system specification for integrated transceiver circuits in accordance with one or more embodiments of the invention.

FIG. 19A-19B shows test data for an integrated transceiver circuit in accordance with one or more embodiments of the invention.

DETAILED DESCRIPTION

Specific embodiments of an integrated electron spin resonance (ESR) spectrometer will now be described in detail with reference to the accompanying figures. Like elements in the various figures (also referred to as FIGs.) are denoted by like reference numerals for consistency.

In the following detailed description of embodiments, numerous specific details are set forth in order to provide a more thorough understanding of integrated ESR spectrometer. However, it will be apparent to one of ordinary skill in the art that these embodiments may be practiced without these specific details. In other instances, well-known features have not been described in detail to avoid unnecessarily complicating the description.

In general, embodiments of the invention relate to an integrated ESR spectrometer. As used herein, the term integrated refers to a monolithic circuit that is integrated onto a single chip substrate. Furthermore the term chip substrate is used herein broadly to include any layer of a multi-layer integrated circuit. For example, one or more embodiments of an integrated ESR spectrometer include a transmitter, receiver, and a programmable pulse generator that are formed on the same chip substrate, e.g., the circuitry may be implemented in silicon by way of a 0.13 μm SiGeBiCMOS process, or the like. In accordance with one or more embodiments, the integrated transceiver of the ESR spectrometer disclosed herein is capable of operating in a continuous wave (CW) mode and/or a pulse mode. In accordance with one or more embodiments, the integrated ESR spectrometer may include also include an integrated ESR probe that employs an integrated resonator for exciting and receiving ESR signals from a sample under test. In accordance with one or more embodiments, the integrated ESR spectrometer may also include an external ESR probe that employs an external resonator for exciting and receiving ESR signals from a sample under test.

In accordance with one or more embodiments, the integrated ESR transceiver chip includes an integrated programmable pulse generator that may produce RF pulses having varying durations and spacings. Programmable pulse durations are possible that have durations that range from 0.5 ns to 500 ns. In addition, the integrated transmitter circuit of the integrated ESR transceiver chip may be switched off very quickly, e.g., in approximately 1 ns. This results in a spectrometer that has a very short, approximately 1 ns, dead time. As used herein, the term spectrometer dead time refers to the minimum duration of time that must elapse between excitation and detection of the ESR signal form the sample.

This programmable pulse capability in combination with this short dead time allows the integrated ESR spectrometer to be used for time domain ESR spectroscopy as well as frequency domain ESR spectroscopy. Furthermore, the integrated ESR system may be used across a number of different frequency ranges. For example, one or more embodiments disclosed herein operate within a range of about 0.5-27 GHz. However, other frequency ranges may be used without departing from the scope of the present disclosure.

Furthermore, as used herein the terms ESR and EPR are understood to be completely synonymous and interchangeable and thus, the use of one or the other is meant to differentiate between the magnetic property of the sample under test. In other words as used herein the terms EPR and
ESR are not meant to limit the type of electronic magnetic property of the sample, but rather are used generally to refer to the a measurement technique that manipulates the electronic magnetization of a sample. As used herein the term magnetic species is used broadly to cover all molecules, atoms, or particles with unpaired electron spins and thus, refers to all species that having a net electronic magnetic moment. Examples of magnetic species include but are not limited to para- or dia-magnetic atoms, molecules, ions, free radicals, or any type of paramagnetic nanoparticle, or any other magnetic particle that may be used to produce an ESR signal. Accordingly, the term EPR and ESR signal as used herein refers to a signal that originates from the magnetic resonance of the species’ electronic magnetic moment (or equivalently the net electronic angular momentum, spin or otherwise) of the species.

The integrated ESR spectrometer in accordance with one or more embodiments may be used to measure ESR parameters such as the spin-spin relaxation time ($T_2$) using RF pulse sequences having two or more RF pulses. In addition, the integrated ESR spectrometer may be used to measure ESR parameters such as the spin-lattice relaxation time ($T_1$) using inversion recovery techniques. In general, the integrated ESR spectrometer may be used to make any other type of time domain ESR measurement without departing from the scope of the present disclosure. In addition, by operating in CW mode, the integrated ESR spectrometer may be used to conduct frequency domain ESR spectroscopy.

In accordance with one or more embodiments, the integrated ESR spectrometer in accordance with one or more embodiments is extremely versatile and may be used in a number of different applications. Because of its small size, e.g., 1 mm by 2 mm, the integrated ESR transceiver chip may be employed in a non-invasive, point-of-care (POC) instrument. For example, integrated ESR spectrometer may be part of a handheld ESR system that may be used to study the properties of magnetic species such as metal ions in enzymes and/or free radicals involved in biochemical signaling pathways. In addition, the ESR system may be used to make direct measurements of the partial pressure of oxygen ($pO_2$) in tissues with high sensitivity and accuracy. Because $pO_2$ has been shown to be related to many diseases, e.g., cancer and peripheral vascular insufficiency, the ESR system in accordance with one or more embodiments may be used to diagnose disease. Furthermore, the integrated ESR spectrometer may be used to diagnose other diseases whose presence may be detectable using ESR, e.g., melanoma. In accordance with one or more embodiments, the integrated ESR system may be used to image free radicals and perform oximetry. Furthermore, one or more embodiments of the invention may employ an active feedback system for increasing the magnitude of the ESR signal. Accordingly, the term EPR and ESR signal as used herein refers to all species that having a net electronic magnetic moment (or equivalently the net electronic angular momentum, spin or otherwise) of the species.

FIGS. 1A-1B further show that the ESR probe module 105 may include a magnet 111 that generates a bias magnetic field $B_0$, that is capable of being varied, e.g., capable of being modulated at a frequency $f_{RF}$. In accordance with one or more embodiments, the magnet 111 may be a solenoid electromagnet having a spatially uniform $B_0$ across the sample. Furthermore, a sample 113 may be located within the magnetic file $B_0$ of the magnet 111. The probe module 105 further includes the resonator 109 that may serve as a resonator for transmitting and receiving RF signals. In accordance with one or more embodiments, the resonator 109 may be integrated into the transceiver chip 100, e.g., in the form of a planar loop-gap resonator as described in more detail below in reference to FIGS. 7A-7B. While a single resonator 109 is shown here for simplicity, one or more embodiments of the invention may employ two or more resonators 109 that are also integrated onto the substrate 100. Such a configuration may or may not employ a circulator 107. When a circulator 107 is employed, the RF path 121, defined as the signal path from the transmitter to the resonator 109 that passes through ports 1 and 2 on the circulator 107, may be isolated from the ESR signal path 123, defined as the signal path from the resonator to the receiver that passes through ports 2 and 3 on the circulator 107. Furthermore, one or more embodiments of the invention may employ an active feedback system for increasing the isolation between the RF path 121 and the ESR signal path 123, thereby reducing the amount of RF leakage power from the transmitter that is detected by the receiver during detection. For example, during CW operation, RF leakage may occur between ports 1 and 3 of the circulator 107.

In an ESR measurement in accordance with one or more embodiments, the magnetic field $B_0$ is also referred to herein as the Zeeman field, may be generated by the magnet 111. As shown in FIGS. 1A-1B, this Zeeman field is present in both the CW and pulsed ESR measurements. The presence of $B_0$ in the sample volume introduces an energy difference $\Delta E$ between the spin states of the unpaired electron(s) in the sample 113. The energy difference $\Delta E$ between the spin states is proportional to both $B_0$ and $g$, where $g$ is the g-factor, a physical parameter that is dependent on the electromagnetic microenvironment surrounding the unpaired electron. Furthermore, the sample 113 may be placed within the sample region of the resonator 109 so that the sample 113 is exposed to the oscillating $B_0$ field generated by the resonator 109. When operating near the resonance frequency $f$ of the resonator 109, the resonator produces a strong RF magnetic field $B_0$ that is perpendicular to $B_0$. In accordance with one or more embodiments, the resonance frequency $f$ is chosen such that $hf=\Delta E$, where $h$ is Planck's constant. Thus, electron transitions between the
spin states are possible and the RF energy generated by the resonator 109 is absorbed efficiently.

FIG. 1A shows an ESR system configured to operate in the CW mode in accordance with one or more embodiments. In the CW mode, a sinusoidal RF signal 115 is sent to the resonator 109 and reflected RF power 117 that is reflected from the resonator is measured to calculate the amount of the RF power absorbed by the sample 113. The absorbed power varies with the strength of the B₀ field and thus, the RF power absorption curve, reflected in the reflected RF power 117 as a function of B₀, reveals magnetic properties of the sample 113. In accordance with one or more embodiments, in order to reduce the low frequency noise (1/f), B₀ may be modulated at a frequency f₀ and the reflected power 117 may be measured at the same modulation frequency f₀. Furthermore, in accordance with one or more embodiments, the B₀ field may be held constant and the RF frequency of the sinusoidal RF signal 115 may be modulated to perform the CW measurement.

FIG. 1B shows an ESR system configured to operate in the pulse mode in accordance with one or more embodiments. In pulse mode, the transmitter circuit 119 sends a sequence of RF pulses 119 to the resonator 109 to manipulate the direction of the spins of unpaired electrons of the sample 113. For example, in a spin echo measurement, a first RF pulse having a length T may flip the spins 90 degrees about B₀. After the RF flip, the sample may emit a free induction decay signal due to the de-phasing of the spins of the sample, which are now precessing, i.e., rotating, about the B₀. Additional pulses having a duration of 2 T that flips the spins by 180 degrees refocuses the de-phased spins and may cause one or more spin echo signals to be emitted from the sample. This ESR signal, in the form of a spin echo signal, is emitted by the sample 113 and received by the resonator 109, now operating as a reception resonator. The ESR signal then travels to the receiver circuit 103 by way of the ESR signal path 123. By applying a properly timed sequence of RF pulses, the timing of and number of detected spin echoes can be controlled. Of course, one of ordinary skill having the benefit of this disclosure will recognize that any type of pulsed ESR measurement may be employed without departing from the scope of the present disclosure. In accordance with one or more embodiments, the receiver circuit 205 of the integrated ESR transceiver chip is configured to receive the ESR signal from the sample by way of the resonator 211a (211b) which may be configured in full duplex mode using a circulator as described above in reference to FIGS. 1A-1B. In other embodiments, the resonator 211a (211b) may include two or more resonators that are designed as dedicated transmitter and receiver resonators. An example of this type of multi-resonator design is shown in FIGS. 12A-12B. In accordance with one or more embodiments, the receiver circuit 205 includes a receiver amplifier circuit 217 that is electrically connected to a mixer circuit 219 that is itself electrically connected to both the oscillator 213 of transmitter circuit 203 and a baseband amplifier circuit 221. In accordance with one or more embodiments, the receiver circuit 205 may be implemented as a low noise amplifier (LNA). However, the receiver amplifier circuit need not be limited by a precise noise figure (NF) and, depending on the design constraints, the required noise figure may vary without departing from the scope of the present disclosure. In accordance with one or more embodiments, the mixer circuit receives an amplified ESR signal from the LNA circuit and converts the amplified ESR signal to a baseband signal that may be subsequently amplified by the baseband amplifier circuit 221. In accordance with one or more embodiments, the amplified baseband signal may be sent to a data acquisition system (DAQ) (not shown) for further processing, storage, and/or display.

In accordance with one or more embodiments, the transceiver chip 201 further includes an integrated programmable pulse generating (PPG) circuit 219 that is fabricated on the same chip substrate 209 as the transmitter circuit 203 and the receiver circuit 205. In other embodiments, the resonator 211a may be optionally fabricated on the same substrate 209 as the transmitter circuit 203 and the receiver circuit 205. In other embodiments, the resonator 211b may be physically separable from the transceiver chip 201, e.g., the resonator 211b may be a flat loop-gap resonator made using a printed circuit board (PCB) such as a 20 mil Rogers 4350 B PCB, e.g., as shown in FIG. 7B. In either case, the transmitter circuit 203 includes an oscillator circuit 213 electrically connected to a power amplifier (PA) circuit 215. In accordance with one or more embodiments, the oscillator circuit 213 is configured to generate an oscillating output signal, which is referred to herein as a power amplifier that is then amplified by the PA circuit 215 and output by the PA circuit 215 as an amplified oscillating output signal. The amplified oscillating output signal is then provided to the resonator 211a (211b) for use in an ESR measurement, e.g., the pulsed or CW measurement as described in more detail above in reference to FIGS. 1A-1B. Accordingly, the amplified oscillating output signal is applied to a sample 212 in order to manipulate the electronic magnetic moments (or spins) of the sample 212 thereby causing an ESR signal that is detectable by the resonator 211a (211b). In one embodiment, the ESR signal may be in the form of a reduction in the amplified oscillating output signal that is reflected from the resonator 211a. In another embodiment, the response may be in the form of an ESR signal that is radiated, or emitted, from the sample and later detected by the resonator 211a (211b), e.g., the ESR signal may be a free induction decay signal, an inversion recovery signal, a spin echo signal, or any other type of ESR signal.

In accordance with one or more embodiments, the receiver circuit 205 of the integrated ESR transceiver chip is configured to receive the ESR signal from the sample by way of the resonator 211a (211b) which may be configured in full duplex mode using a circulator as described above in reference to FIGS. 1A-1B. In other embodiments, the resonator 211a (211b) may include two or more resonators that are designed as dedicated transmitter and receiver resonators. An example of this type of multi-resonator design is shown in FIGS. 12A-12B. In accordance with one or more embodiments, the receiver circuit 205 includes a receiver amplifier circuit 217 that is electrically connected to a mixer circuit 219 that is itself electrically connected to both the oscillator 213 of transmitter circuit 203 and a baseband amplifier circuit 221. In accordance with one or more embodiments, the receiver amplifier circuit may be implemented as a low noise amplifier (LNA). However, the receiver amplifier circuit need not be limited by a precise noise figure (NF) and, depending on the design constraints, the required noise figure may vary without departing from the scope of the present disclosure. In accordance with one or more embodiments, the mixer circuit receives an amplified ESR signal from the LNA circuit and converts the amplified ESR signal to a baseband signal that may be subsequently amplified by the baseband amplifier circuit 221. In accordance with one or more embodiments, the amplified baseband signal may be sent to a data acquisition system (DAQ) (not shown) for further processing, storage, and/or display.

In accordance with one or more embodiments, the transceiver chip 201 further includes an integrated programmable pulse generating (PPG) circuit 219 that is fabricated on the same chip substrate 209 as the transmitter and receiver circuits. Furthermore, the PPG circuit 219 may be electrically connected to the PA circuit 215 and/or the oscillator circuit 213 and configured to switch the output of the transmitter circuit 203 by switching the oscillator circuit 213 and/or the PA 215, e.g., to perform pulsed ESR experiments. One or more embodiments of the integrated programmable pulse generating (PPG) circuit is shown in FIG. 3. The PPG circuit 301 is capable of producing digital pulses with pulse widths ranging from 0.5 ns-500 ns and is integrated onto the chip substrate along with the transmitter and receiver circuits as shown, e.g., in the micrographs of FIG. 6A and FIG. 11A. In accordance with one or more embodiments, the pulse width is determined by the time it takes for the capacitor 305 to discharge from the supply voltage VDD.
to a threshold voltage. The “Set” signal 307 is derived from an external clock signal and charges the capacitor 305 on falling edges through the pull-up PMOS transistor 309 and discharges the capacitor 305 through the current sources 311a, 311b, 311c, . . . 311n on rising edges. In accordance with one or more embodiments, ten binary scaled current sources may be used, each representing a digital bit, to control the rate at which the capacitor discharges and therefore control the pulse width. However, any number of current sources may be used without departing from the scope of the present disclosure. In accordance with one or more embodiments, the pulse width can be adjusted with a resolution of 490 ps. In accordance with one or more embodiments, the discharge path through the current sources is controlled using a double switch design that employs a first set of switches 317a, 317b, 317c, . . . 317n controlled by the set signal and a second set of switches B[0], B[1], B[2], . . . B[n] that are used to control the number of current sources used for the discharge path, thereby setting the pulse width.

Furthermore, the PPG 301 employs a comparator-NOR logic gate on the output that includes comparator 311 coupled to NOR gate 315. Test data showing output pulses of the PPG relative to the clock signal is shown in FIGS. 13A-13B. As seen from the data in FIG. 13B, the PPG can output pulses ranging from a few ns to a few hundred ns.

In what follows, FIGS. 4-8 describe an integrated ESR system in accordance with one or more embodiments of the invention. In these embodiments, the system is designed to operate in both pulsed and CW modes and to operate over a frequency range of 770 MHz to 970 MHz. Such a system may be implemented, e.g., in a handheld device and may be used in a wide range of non-invasive point-of-care (POC) applications, e.g., to image free radicals and/or perform oximetry. In accordance with one or more embodiments, the ESR system may be implemented as shown in FIG. 2 using an integrated ESR transceiver chip connected to an external resonator.

FIGS. 4A-4B show an integrated transmitter circuit in accordance with one or more embodiments of the invention. FIG. 4A shows a diagram of a transmitter circuit 401 that is suitable for an ESR spectrometer in accordance with one or more embodiments of the invention. The transmitter circuit 401 includes a voltage controlled oscillator circuit (VCO) 403, a VCO buffer circuit 405, an RF buffer circuit 407, and a power amplifier circuit (PA) 409. In accordance with one or more embodiments, the VCO 403 provides an oscillating signal having a voltage tunable frequency. The output of the VCO 403 is buffered by the VCO buffer circuit 405 and the RF buffer circuit 407. In accordance with one or more embodiments, the VCO buffer circuit 405 ensures that the oscillation frequency of the VCO 403 remains unchanged by keeping the VCO 403 load impedance constant during the transition from excitation phase (PA on) to detection phase (PA off). In this example, the VCO buffer circuit 405 is located between the output of the VCO 403 and the LO input of a mixer (not shown) used in the receiver, as described in more detail below. In accordance with one or more embodiments, the output of the transmitter circuit 401 is switched by switching the PA circuit 409 rather than switching the VCO. Furthermore, the switching of the PA circuit 409 is accomplished not by switching V_{DS}, but rather, by pulling down the bias voltage of an input transistor of the PA as described in more detail below in reference to FIG. 4B.

Accordingly, the oscillating output signal of the transmitter may be very quickly turned on and off, i.e., it may be pulsed by providing pulses to the PA from the on-chip PPG, e.g., the PPG shown in FIG. 3. In accordance with one or more embodiments, the integrated transmitter may be switched in approximately 1-2 ns, thereby enabling pulsed ESR experiments to be performed with the system.

FIG. 4B shows the topology of an integrated transmitter circuit like that shown in FIG. 4A in accordance with one or more embodiments of the invention. VCO circuit 403 is connected to the PA circuit 409 that may be implemented on the ESR transceiver chip in accordance with one or more embodiments. The VCO circuit 403 adopts a fully differential negative resistance structure with an LC tank. The frequency of this VCO is determined by the LC tank resonance frequency. The application of a voltage V_{tune} to the tuning terminal 413 of the VCO results in a frequency that can be tuned from 770 MHz to 970 MHz, as shown in the test data of FIG. 14A. In accordance with one or more embodiments, the frequency is tuned by applying V_{tune} as a bias voltage on the two varactors 415 and 417 that are placed in parallel with the LC tank. A symmetric inductor 419 is used to improve the symmetry of the device. As the PN junction capacitance reduces for an increasing negative bias, the VCO frequency will be increased as V_{tune} increases. However, because the capacitance of varactors 415 and 417 are comparatively small, parallel fixed value capacitors 421 and 423 are used to further bring down the frequency to approximately 1 GHz. In accordance with one or more embodiments, the VCO signal is amplified by a differential buffer circuit 425 and is converted to a single-ended signal by signal converter 427. FIG. 4C shows one example of an integrated signal converter circuit 427 in accordance with one or more embodiments. The single-ended VCO signal is then fed to an on-chip PA circuit 409 for additional amplification. In accordance with one or more embodiments, the on-chip PA circuit 409 has a cascode topology and provides a power gain of 15 dB. Furthermore, the output of the PA is matched to 50Ω by a combination of on-chip inductors and capacitors 429. While the VCO shown in FIG. 4B employs a fully differential negative resistance structure with an LC tank, any type of VCO structure may be employed without departing from the scope of the present disclosure. Likewise, while the PA shown in FIG. 4B employs a single-ended cascode structure, any type of PA structure may be employed without departing from the scope of the present disclosure.

In accordance with one or more embodiments, the transmitter circuit 401 may be operated in both CW and pulsed mode. Because the time scale for tuning off the VCO 403 is too slow for the demanding speed requirements of pulsed ESR, the transmitter circuit 401 in the integrated ESR transceiver is switched by switching off the PA circuit 409 while leaving the VCO 403 in the on state. In accordance with one or more embodiments, the PA circuit 409 may be turned off by pulling down the base voltage of its input transistor 431 using an N-channel metal-oxide-semiconductor field effect transistor (NMOSFET) driver 435. Generally speaking, for a pulse mode ESR spectrometer, the speed at which the transmitter may be switched off determines the dead time of the spectrometer (i.e., the minimum wait time before which ESR signals may be received from the sample). Since the ESR signal is usually much weaker than the RF excitation signal, it can only be detected after switching off the transmitter circuit 401. The amplitude of the ESR echo decays exponentially with wait time, and therefore, a small turn-off time is extremely important in the pulsed mode measurements. However, by employing the design shown in FIG. 4B, the transistor may be switched off very quickly by using a high speed pull down circuit formed from the NMOSFET driver 435. In this example, the NMOSFET driver 435 is used to quickly pull down the base
voltage of the input transistor \( V_{pulse} \). More specifically, when \( V_{pulse} \) outputs a low voltage (e.g., approximately 0.1 V), the transistor \( 431 \) is off. Therefore, the bias of transistor \( 431 \) depends only on the voltage \( V_{pulse} \) and the PA is in the on state. Then, if \( V_{pulse} \) is a high voltage (e.g., approximately 1 V), transistor \( 435 \) is turned on and thus, reduces the bias of transistor \( 431 \). The size of transistor \( 435 \) is chosen so that when transistor \( 435 \) is on, the bias of transistor \( 431 \) is close to 0 V and well below the threshold voltage of transistor \( 431 \). Accordingly, in the one or more embodiments that employ the switching design shown in FIG. 4B, the transmitter may be turned off in less than 1.2 ns thereby facilitating pulsed ESR measurements to be made using the integrated ESR transceiver chip. FIG. 15 shows test data for a turn off characteristic of the transmitter circuit \( 401 \) in accordance with one or more embodiments.

FIG. 5A shows an example of an integrated receiver circuit that may be employed as the receiver circuit in an integrated ESR transceiver chip in accordance with one or more embodiments. The receiver circuit \( 501 \) includes a low noise amplifier circuit (LNA) \( 503 \), a mixer circuit \( 505 \), and a baseband amplifier circuit \( 507 \). In accordance with one or more embodiments, the input of the LNA circuit \( 503 \) is electrically connected to the resonator (not shown) and receives an ESR signal from sample (not shown) that is located in, or near, the resonator. The output of the LNA circuit \( 503 \) is electrically connected to the RF input port of the mixer circuit \( 505 \). Furthermore, as described above, the LO input port of the mixer circuit \( 505 \) is electrically connected to the VCO thereby providing the LO signal for the down conversion of the ESR signal to the baseband frequency. Furthermore, the IF output port of the mixer is electrically connected to the input terminal of the baseband amplifier circuit \( 507 \). Thus, after being amplified by the LNA circuit \( 503 \), the ESR signal is down-converted to a baseband frequency and the baseband signal is then amplified by the baseband amplifier circuit \( 507 \). In accordance with one or more embodiments, the amplified baseband signal may be output to a data acquisition system (DAQ) (not shown). In accordance with one or more embodiments, any type of data acquisition system may be used without departing from the scope of the present disclosure.

FIG. 5B shows the topology of an integrated receiver circuit like that shown in FIG. 5A in accordance with one or more embodiments. The direct-conversion architecture is adopted that includes LNA circuit \( 503 \), mixer circuit \( 505 \), and baseband amplifier circuit \( 507 \). The ESR signal from the sample is coupled to the input \( 509 \) of the LNA circuit \( 503 \). This signal is down-converted by the mixer circuit \( 505 \) and amplified by the baseband amplifier circuit \( 507 \). This amplified baseband signal is then sent to the DAQ for analysis. In accordance with one or more embodiments, the LNA circuit \( 503 \) has three stages and it is designed to have a power gain of 40 dB and a noise figure of 3.6 dB over the entire frequency range of the VCO. The LNA output 1 dB compression point is \(-15\) dBm. Furthermore, in the physical layout of the LNA, a guard-ring with substrate contact may be used to prevent the substrate coupling from the transmitter to the receiver. While a three stage LNA is shown here as an example, one of ordinary skill will appreciate that any number of stages and topologies may be used for the LNA without departing from the scope of the present disclosure.

In accordance with one or more embodiments, the mixer circuit \( 505 \) has a Gilbert topology with a resistive load, as shown in FIG. 5A. In accordance with one or more embodiments, because the LNA is single-ended, only one transistor \( 511 \) in the mixer takes the output of the LNA and the other transistor \( 513 \) is tied to the same DC voltage. In accordance with one or more embodiments, the mixer may feed to a two stage baseband amplifier circuit \( 507 \). In a CW ESR measurement, the ESR signal after the mixer has a low frequency in the kHz domain and thus, DC block capacitors cannot be used after mixer for biasing purposes. Therefore, the first stage of the baseband amplifier may be a differential source-follower that serves to shift the DC voltage of the mixer output. The second stage may then be a common source amplifier with output matched to \( 507 \). While the mixer shown in FIG. 5B employs the Gilbert topology with a resistive load, any type of mixer topology may be employed without departing from the scope of the present disclosure. Likewise, any topology for the baseband amplifier may be employed without departing from the scope of the present disclosure.

In accordance with one or more embodiments, the integrated ESR transceiver chip includes an integrated PPG as shown in FIG. 3, an integrated transmitter as shown in FIGS. 4A-4B, and an integrated receiver as shown in FIGS. 5A-5B, all located on the same chip substrate. As mentioned above, each of these components may be implemented in silicon, e.g., by way of a 0.13 µm SiGeBiCMOS process, or the like.

To that end, FIG. 6A shows a micrograph of the fabricated integrated ESR chip that includes the on-chip transmitter (VCO, buffer, and PA), receiver (LNA and mixer), and PPG circuits described above in reference to FIGS. 1-5. In this example the chip size is 2.5 mm by 1.5 mm and the power consumption of the entire chip is less than 425 mW. In addition, FIGS. 6B-6H show one example of a layout of an integrated ESR transceiver chip, from top layer to bottom layer, respectively. FIG. 6A shows a micrograph of one example of a fabricated integrated transceiver chip in accordance with one or more embodiments having a size of 2.5 mm by 1.5 mm.

Furthermore, FIGS. 13-19 summarize test data and operational specifications of an integrated ESR transceiver chip shown in FIG. 6. FIG. 14A shows the measured tuning range data for the VCO described above in FIG. 4B and implemented as shown in the micrograph of FIG. 6A. FIG. 15 shows a measured turn off characteristic for the transmitter described in FIG. 4B that proves that the transmitter may be switched off in approximately 1 ns. FIG. 16 shows measured output pulse data for the transmitter described in FIG. 4B operating in pulse mode.

As briefly described above, the integrated ESR transceiver chip may be employed as part of an ESR spectrometer system in accordance with one or more embodiments. FIG. 7A shows a more detailed diagram of an ESR spectrometer 701 that employs an integrated ESR transceiver chip 705 like the one described above in reference to FIGS. 2-6. In accordance with one or more embodiments, the system 701 includes a receiver circuit 723, a DAQ 711, a circulator 713, and an ESR probe module 715. The interaction of these components is described in detail above in reference to FIG. 1A-1B. As already described in detail above, the ESR transceiver chip 703 includes an integrated PPG circuit 705, an integrated transmitter circuit 707, and an integrated receiver circuit 709. Furthermore, as described above, the converted baseband signal is output to DAQ 711. In accordance with one or more embodiments, ESR probe 715 of the ESR system 701 may be external to the ESR transceiver chip 703. Furthermore, in accordance with one or more embodiments, the output signal from the transmitter circuit 707 may be sent to a planar loop-gap resonator 725 via the circulator 713. A planar loop-gap resonator 725 in accordance with one
or more embodiments is shown in FIG. 7B and may be fabricated on a printed circuit board (PCB), e.g., a 20 mil Rogers 4350B PCB. In this example, the loop has an inner and outer diameter of 4 mm and 5 mm, respectively. In accordance with one or more embodiments, the loaded quality factor Q of the resonator 725 is measured to be 60 and the resonance frequency may be tuned using one or more on-board tunable capacitors. Furthermore, in accordance with one or more embodiments, variable capacitors may be applied in parallel and series with the resonator 725 to tune the resonance frequency and match the input impedance of the resonator 725 to 50Ω. FIG. 7C shows another example of a resonator in accordance with one or more embodiments. More specifically, FIG. 7C shows a split-gap transmission line resonator in accordance with one or more embodiments. Other types of resonators may be used without departing from the scope of the present disclosure.

In accordance with one or more embodiments, the ESR system 701 may operate in pulse or CW mode. In pulse mode, the PPG circuit 705 may be driven by external clock 717. In CW mode, the PPG is set so that the transmitter is in the on-state and then the ESR signal is acquired by modulating the B field using the signal generator 719 to modulate the current of the electromagnet 721 while simultaneously measuring the reflected power from the resonator 725, as described in more detail above in reference to FIG. 1A.

In accordance with one or more embodiments, during the CW measurement, the transmitter circuit 707 and the receiver circuit 723 are both in the on state. However, because a typical circulator 713 has an isolation value of only 20 dB, the leakage power from the transmitter to the receiver (e.g., through leakage from port 1 to port 3 of the circulator 713) may be considerably larger than the ESR signal from the sample. For example, assuming the excitation signal is 0 dBm, the leakage power at the input of the receiver is ~20 dBm, while the ESR signal can be lower than ~110 dBm. Therefore, in order not to saturate the ESR signal, the input referred LNA IIP3 of the LNA must be higher than ~20 dBm, while the LNA still needs to provide high gain in order to reduce the noise contribution of the following stages in the receiver. Accordingly, in order to relax this demanding design specification of the LNA and the receiver, an active cancellation structure may be employed to cancel the leakage power from the transmitter, in accordance with one or more embodiments.

FIG. 8 shows a diagram of the active leakage cancellation circuit 800 in accordance with one or more embodiments. In accordance with one or more embodiments, this active leakage cancellation circuit 800 may be employed using discrete or integrated RF components. In this example, the oscillating output signal from the transmitter circuit 801, which is the integrated transmitter circuit of the integrated ESR transceiver chip, is split to two parts A and B by the power splitter 803. The signal A goes through the circulator 805 and a small portion A’ leaks to the point C. The signal B goes through a variable gain amplifier/attenuator (VGA) 807 and a phase shifter 809, and then arrives at point D. The signal at point C and point D is summed at the summing junction 811 and the summed signal is applied to the input of the receiver circuit 815, which is the integrated receiver circuit of the integrated ESR transceiver chip in accordance with one or more embodiments. A power sensor 813 with high input impedance monitors the power at the input 815a of the receiver, as shown. In accordance with one or more embodiments, the power sensor 813 has a high input impedance so as not to degrade the matching and noise figure of the receiver circuit 815. In accordance with one or more embodiments, two control signals 817 and 819 are generated by the power sensor 813 to tune the VGA 807 and the phase shifter 809 such that the power measured by the power sensor 813 at the input of the receiver circuit 815 is minimized. Thus, the action of the VGA 807 and phase shifter 809 is to provide a signal at point D that has the same amplitude but 180 degree phase difference from the leakage signal A’. The addition of this signal to the leakage signal A’ leads to a destructive interference between the two signals that causes a cancellation of the leakage signal A’ at the input 815a. In accordance with one or more embodiments, the active cancellation circuit 800 may reduce the leakage signal A’ by more than 40 dB as measured at the input 815a.

In what follows, FIGS. 9-13 describe a mm wave ESR system in accordance with one or more embodiments of the invention. In these embodiments, the system is designed to operate in both pulsed and CW modes and to operate over a frequency range of 22 GHz to 26 GHz. Such a system may be implemented, e.g., in a handheld device and may be used in a wide range of non-invasive point-of-care (POC) applications, e.g., for making direct measurements of partial pressure of oxygen (pO2) of tissue and/or to diagnose melanoma. In accordance with one or more embodiments, the ESR system may be implemented as shown in FIG. 2 using an integrated ESR transceiver chip having a resonator that is integrated on-chip.

FIG. 9A shows a diagram of a transmitter circuit 901 that is suitable for an integrated ESR transceiver chip in accordance with one or more embodiments of the invention. The transmitter circuit 901 includes a voltage controlled oscillator (VCO) circuit 903, a VCO buffer circuit 905, a dual stage RF buffer circuit 907, a dual stage LO buffer circuit 911, and a power amplifier (PA) circuit 909. In accordance with one or more embodiments, the VCO circuit 903 provides an oscillating signal having a voltage tunable frequency. The output of the VCO circuit 903 is buffered by the VCO buffer circuit 905 and the dual stage RF buffer circuit 907. In accordance with one or more embodiments, the VCO buffer circuit 905 ensures that the oscillation frequency of the VCO circuit 903 remains unchanged by keeping the VCO circuit 903 load impedance constant during the transition from excitation phase (PA on) to detection phase (PA off). In accordance with one or more embodiments, the VCO buffer circuit 905 is located between the output of the VCO circuit 903 and the input of the dual stage LO buffer circuit 911. The output of the dual stage LO buffer circuit 911 is connected to the LO input of the mixer (not shown) used in the receiver, as described in more detail below. Furthermore, in this example, the dual stage RF buffer circuit 907 is located between the output of the VCO buffer circuit 905 and the input of the PA circuit 909. In accordance with one or more embodiments, in order to improve switching speed and switching isolation, the output of the transmitter circuit 901 is switched by switching the PA circuit 909 along with the second stage of the dual stage RF buffer circuit 907 rather than switching the VCO circuit 903. Furthermore, the switching of the PA circuit 909 is accomplished not by switching VDD but rather by employing NMOSFET switches connected to the biasing nodes of the PA. In accordance with one or more embodiments, the NMOSFET switches act as a high-speed pull-down circuit, as described in more detail below. By switching the PA in this manner, the oscillating output signal of the transmitter may be very quickly turned on and off, i.e., it may be pulsed by providing pulses to the PA from the on-chip PPG, e.g., the PPG shown in FIG. 3. In accordance with one or more embodiments, the
integrated transmitter may be switched in approximately 1-2 nanoseconds, thereby enabling pulsed ESR experiments to be performed. Furthermore, by switching in this manner, isolation between the transmitter and receiver circuits of the integrated ESR transceiver chip may be improved.

FIGS. 9B-9D shows the topology of a transmitter circuit that is shown in FIG. 9A in accordance with one or more embodiments of the invention. The transmitter circuit 901 includes a voltage controlled oscillator (VCO) circuit 903, a VCO buffer circuit 905, both shown in FIG. 9B; a dual stage RF buffer circuit 907a and 907b, both shown in FIG. 9C; a dual stage LO buffer circuit 911a and 911b, both shown in FIG. 9D, and a power amplifier (PA) circuit 909 shown in FIG. 9B. In accordance with one or more embodiments, the VCO topology used is a negative resistance cross-coupled transistor pair that provides the oscillator core. Differential transistors are used to bias the oscillator core as well as to serve as an inductor to resonate with the VCO varactors, which are implemented using reverse-biased diodes. The VCO is followed by a single-stage buffer that isolates the VCO from the PA and its preamplifier. The VCO signal is then routed to the RF and the LO paths, each through a two-stage buffer. In particular, the second stage 907b of the two-stage buffer in the RF path has a switches 917a, 917b that short its base voltage to ground, providing a high level of isolation between the VCO and the detection coil. The PA has a similar switching mechanism through base pull-down transistors. More specifically, fast switching is achieved through employing NMOSFET switches 915a, 915c, respectively, of the PA. Accordingly, the NMOSFET switches act as a high-speed pull-down circuit. This high speed pull down circuit operates in a manner that is identical to that described above in reference to the pull down circuit of FIG. 4. In addition, switching the PA in this manner provides further isolation between the detection coil (not shown) and the VCO signal. This operation allows for the VCO to remain on throughout all stages, eliminating start-up time issues. The combined effect of switching the buffer 907b and the PA 909 results in a 55 dB on/off ratio for the current on the excitation coil.

FIG. 10A shows an example of an integrated receiver circuit that may be employed as the receiver circuit in an integrated ESR transceiver chip in accordance with one or more embodiments. The receiver circuit includes a low noise amplifier (LNA) circuit 1001, a mixer circuit 1005, and a baseband amplifier circuit 1007. In accordance with one or more embodiments, the input of the LNA circuit 1003 is electrically connected to the resonator (not shown) and receives an ESR signal from sample (not shown) that is up-converted to the baseband frequency and the baseband signal is then amplified by the baseband amplifier circuit 1007 and output to a data acquisition system (DAQ) (not shown). In accordance with one or more embodiments, any type of data acquisition system may be used without departing from the scope of the present disclosure.

FIGS. 10B-10C show the topology of an integrated receiver circuit like that shown in FIG. 10A in accordance with one or more embodiments of the invention. The receiver circuit includes four-stage variable-gain LNA circuit 1003, shown in FIG. 10B; and mixer circuit 1005 and baseband amplifier circuit 1007, shown in FIG. 10C. The ESR signal from the sample is coupled to the input 1009 of the LNA circuit 1003. This signal is down-converted by the mixer circuit 1005 and amplified by the baseband amplifier circuit 1007. This amplified baseband signal is then to the DAQ for analysis. In accordance with one or more embodiments, the LNA circuit 1003 is a four-stage variable-gain LNA providing a maximum voltage gain of 61 dB. Each stage of the LNA uses a differential cascode topology. The LNA input matching circuit is designed to maximize the LNA gain and to provide a match to the detection resonator coil (not shown). In accordance with one or more embodiments, the baseband amplifier includes a differential stage matched to a differential output impedance of 100Ω.

In accordance with one or more embodiments, the integrated ESR transceiver chip may include an integrated PPG as shown in FIG. 3, an integrated transmitter as shown in FIGS. 9A-9D, and an integrated receiver as shown in FIG. 10A-10C all located on the same chip substrate. As mentioned above, each of these components may be implemented in silicon, e.g., by way of a 0.13 µm SiGeBiCMOS process, or the like. To that end, FIG. 11A shows a micrograph of the fabricated integrated ESR chip that includes the programmable pulse generator, as described in FIG. 3, the on-chip transmitter (VCO, VCO buffer, two-stage RF buffer, two-stage LO buffer, and PA), receiver (4-stage LNA, mixer, and BB amplifier), and an integrated (on-chip) resonator. In this example the chip size is 2 mm by 1 mm and the power consumption of the entire chip is less than 385 mW. In addition, FIGS. 11B-11H shows the layout of the layers of the chip, from top layer to bottom layer, respectively, fabricated as shown in the micrograph of FIG. 11A. Furthermore, FIGS. 14-18 summarize test data and system specifications of an integrated ESR transceiver chip like the one shown in FIG. 11. FIG. 14B shows measured tuning range data for the VCO described above in FIG. 9B and implemented as shown in FIG. 11A. As briefly described above with reference to FIG. 2, the integrated ESR transceiver chip may be employed as part of an ESR spectrometer system in accordance with one or more embodiments. FIGS. 12A-12B show a more detailed diagram of an ESR spectrometer 1201 that employs an integrated ESR transceiver chip 1203 like the one described above in reference to FIGS. 9-10. The functional details of an integrated ESR system have already been described above in reference to FIGS. 1A-1B and FIG. 7 and will not be reproduced here. However, the integrated ESR system shown in FIGS. 12A-12B differs from that described, e.g., in FIG. 7 because it employs an integrated resonator 1200 that includes a transmitter coil 1200a and a receiver coil 1200b. As already described in detail above in reference to FIGS. 9-10, the ESR transceiver chip 1203 includes an integrated transmitter circuit 901 and an integrated receiver circuit 1001. In this example, integrated ESR system includes
external electromagnet 1211 for providing B₀. A sample 1213 may be located near the integrated resonator 1200.

FIG. 12B shows a more detailed view of the elements of the integrated ESR system in accordance with one or more embodiments. In this example, the PA circuit 1215 of the transmitter circuit converts the input RF power from the VCO to a current in the transmitter coil 1200a. This current generates the RF magnetic field pulse (B₁ pulse) that may be used to manipulate the spins of the unpaired electrons in the sample. After the B₁ pulse, the PA and its pre-driver buffer are switched off to allow the receiver circuit 1209 to sense the ESR signal. In accordance with one or more embodiments, the PA may employ an output matching network that is optimized using on-chip transmission lines. In accordance with one or more embodiments, the top metal layers having relatively low sheet resistances (0.007Ω/□ for AM and 0.37Ω/□ for MQ) may be used for the ESR resonator coils 1200a and 1200b in order to maximize the quality factor of the resonator. Furthermore, the coil size may be 20 µm and thus, the coil may produce a B₁ field of 20 G with an excitation current of 16 mA. Like the system described above in reference to FIG. 7, in accordance with one or more embodiments, the ESR system shown in FIGS. 12A-12B may operate in pulse or CW mode.

FIG. 19A shows an example ESR spectrum obtained using the CW ESR method as described above with a 50 mM room temperature sample of 2,2-diphenyl-1-picrylhydrazyl (DPPH), which is a powder composed of stable free-radical molecules commonly used as a standard for position and intensity of ESR measurements. In this measurement, the Zeeman magnetic field B₀ is swept from 330 G to 352 G. The VCO frequency is kept constant at 954 MHz, which is the resonance frequency of the loop-gap resonator in this example. In this example, the integrated transmitter sent an optimum power of 2 dBm to the resonator without saturating the ESR signal. This amount of RF power generates about 0.6 G magnetic field at the center of the resonator. B₁ is further modulated by a 2 kHz signal with 0.27 G amplitude to reduce the Flicker (1/f) noise. The response curve in FIG. 19B is the first-derivative of the Lorentzian absorption line. FIG. 19B shows the results of a similar experiment using Fe₃O₄ nanoparticles.

While the invention has been described with respect to a limited number of embodiments, those skilled in the art, having benefit of this disclosure, will appreciate that other embodiments can be devised which do not depart from the scope of the invention disclosed herein. Accordingly, the scope of the invention should be limited only by the attached claims.

What is claimed is:

1. An integrated electron spin resonance (ESR) circuit chip, the chip comprising:
   a chip substrate;
   a transmitter circuit provided by the chip substrate, the transmitter circuit comprising:
   an oscillator circuit configured to generate an oscillating output signal; and
   a power amplifier (PA) circuit configured to generate an amplified oscillating output signal based on the oscillating output signal;
   a receiver circuit provided by the chip substrate that receives an ESR signal from an ESR probe, the receiver circuit comprising:
   a receiver amplifier circuit configured to receive an amplified ESR signal based on the received ESR signal before down conversion;
10. The integrated ESR spectrometer of claim 8, wherein the resonator is disposed on the chip substrate.

11. The integrated ESR spectrometer of claim 9, further comprising a circulator and an active leakage cancellation circuit configured to cancel a leakage signal that leaks from the transmitter circuit to the receiver circuit by:
   generating a cancellation signal based on an amplitude and a phase of the leakage signal, wherein the cancellation signal has an amplitude that is substantially equal to the amplitude of the leakage signal and a phase difference with the phase of the leakage signal of 180 degrees; and
   adding the cancellation signal to the input of the receiver circuit to cancel the leakage signal.

12. The integrated ESR spectrometer of claim 8, wherein the integrated ESR transceiver chip further comprises:
   an integrated digital pulse generator circuit, wherein the integrated digital pulse generator circuit is disposed on the chip substrate.

13. The integrated ESR spectrometer of claim 12, wherein the integrated digital pulse generator circuit is configured to provide a voltage pulse to a gate terminal of a switching transistor to switch the amplified oscillating output signal.

14. The integrated ESR spectrometer of claim 13, wherein the switching transistor is connected to an input terminal of the PA circuit and the switching transistor is configured to pull down a bias voltage of an input transistor of the PA circuit to switch the amplified oscillating output signal in response to the voltage pulse from the integrated digital pulse generator circuit.

15. The integrated ESR spectrometer of claim 14, wherein the switching transistor is an integrated NMOSFET driver configured to switch off the PA circuit by pulling down the bias voltage of the input transistor of the PA circuit to substantially zero volts.

16. The integrated ESR spectrometer of claim 9, wherein the resonator is a planar loop gap resonator.

17. The integrated ESR spectrometer of claim 10, wherein the resonator comprises a transmitter resonator and a receiver resonator.

18. The integrated ESR spectrometer of claim 17, wherein the transmitter resonator is a planar loop gap resonator.

19. The integrated ESR spectrometer of claim 17, wherein the receiver resonator is a planar loop gap resonator.

20. The integrated ESR spectrometer of claim 17, wherein the transmitter resonator is a transmission-line based resonator.

21. The integrated ESR spectrometer of claim 17, wherein the receiver resonator is a transmission-line resonator.