RICE UNIVERSITY

Sub-picosecond Wireless Synchronization and Instantaneous Frequency Detection for Agile RF/mm-Wave Receivers

by

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Abstract

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Wireless synchronization of a distributed array with widely spaced sparse elements is a key enabler in the coherent combining of signals in space. The angular resolution of an imaging array can be enhanced by increasing the aperture size of the array, which demands a precision synchronization link with a small timing jitter among the array elements. A wireless method for synchronizing multiple chips will ease the scalability of the array. Millimeter-wave Continuous Wave (CW) sources have been used for this purpose, but they usually suffer from high phase and amplitude jitters due to Non-Line-of-Sight (NLOS) reflections caused by time-varying channels in a multi-path environment. In this work, I present a wireless synchronization receiver using sub-8psec pulses. A novel self-mixing technique is introduced to detect low-power picosecond impulses and to extract the repetition rate (1–10 GHz) with a low timing jitter.

Fast spectrum sensing is another key challenge in radio-frequency (RF) systems. Smart reconfigurable systems and sensors that can detect the operating frequency of the received electromagnetic waves are needed for developing cognitive radio systems that can sense used RF channels in the environment and allocate unused frequency bands for their operation. A
frequency detector circuit is a key enabler for the front-end of such systems that can be used to build frequency-locked loops, as well as self-tuned reconfigurable receivers. The output settling time in such circuits needs to be short so that fast spectrum sensing can be achieved for frequency-hopping purpose. A high-speed frequency-to-voltage converter (FVC) is presented here that can detect the instantaneous frequency of the input signal with a 2.6 GHz bandwidth.
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Finally, I thank my parents and my sister for their everlasting love and support.
To My Family: Behrooz, Mina, and Vida
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3.1 Comparison of the presented FVC with prior art. . . . . . . . . . . . 24
Radiating and detecting high-frequency electromagnetic waves using silicon integrated circuits have attracted a great deal of attention in recent years due to the low cost of microchip fabrication in high volumes [1, 2, 3, 4, 5]. Despite the limited operating frequency of integrated transistors, which is characterized by parameters such as $f_T$ and $f_{\text{max}}$, researchers have tried to push the frequency bandwidth of circuits and systems to higher values [6, 7, 8, 9].

Increasing the data rate in communication systems is one potential application of having transceivers that can operate in a wide frequency spectrum [10]. Broadband electromagnetic waves (for example, ultra-short picosecond pulses), also enable secure Line-of-Sight communications. Fig. 1.1 shows the transmission of a short impulse in two cases: Line-of-Sight (LOS) and Non-Line-of-Sight (NLOS). By using multiple transmitter antennas, we can separate the received LOS impulse from the NLOS reflections due to different attenuation and time delays in the two paths [11].

High-resolution three-dimensional imaging systems and high-precision object localization may also be realized using broadband electromagnetic pulses [12, 13, 14]. A high-resolution imaging system consists of an ultra-short impulse radiator and receiver array in which the receivers detect the reflected impulses from the object being
Figure 1.1: Separation of Line-of-Sight signal from NLOS reflections by using ultra-short pulses

tested. In an impulse array, the angular resolution in degrees can be calculated by
\[ \theta = 2\sin^{-1}\left(\frac{c\tau}{D}\right) \]
where \( D \) is the aperture size, \( c \) is the speed of light, and \( \tau \) is the impulse width. The angular resolution of imaging radars is proportional to the inverse of the array size. One way to implement a large array is to separately implement multiple impulse transceiver chips. This demands a tight synchronization among multiple elements of the array, which will be discussed in this thesis.

A broadband signal source and its detector can also be utilized for millimeter-wave and terahertz trace-gas spectroscopy, in which a series of frequency tones separated by the pulse repetition rate enable detection of the absorption frequency of a certain molecular gas. The terahertz (THz) region is a part of electromagnetic spectrum that contains fingerprints of many trace gases. However, due to technical difficulties of designing electrical or optical systems in these frequencies, few spec-
troscopy systems have been built for the THz region [15, 16, 17, 18]. One of the most significant applications of an ultra-short impulse receiver is that it has the ability to detect the absorption lines in the mm-wave and THz region with a high tuning capability.

Finally, the ability to detect the frequency components of an arbitrary incoming signal with an instantaneous method will provide us with the opportunity to build smart reconfigurable systems that have the ability to self-tune in order to receive an arbitrary input. A new method for this purpose will also be discussed in this dissertation that will ease fast spectrum sensing.

1.1 Organization

Chapter 2 describes a novel architecture based on a nonlinear self-mixing method to detect ultra-short picosecond pulses and to extract their repetition rate with a sub-picosecond timing precision. This architecture, along with an on-chip receiving antenna, is implemented in a 130nm SiGe BiCMOS technology; measurement results have demonstrated a 376-fs timing jitter in the synchronized clock.

In chapter 3, a similar problem dealing with frequency detection is studied for the case of continuous-wave (CW) systems. I will introduce the design of an instantaneous frequency-to-voltage converter (FVC) that works for frequencies up to 2.6 GHz. The architecture is based on detecting the first two rising edges of the input signal and charging a main capacitor for one cycle. This circuit has been fabricated in a 90nm IBM CMOS process technology; the measurement results are reported in the same chapter.
Chapter 2

A mm-Wave Impulse Receiver for Sub-picosecond Wireless Synchronization

2.1 Introduction

In this chapter, a sub-8psec impulse receiver is presented to perform low-jitter wireless synchronization. A novel self-mixing technique is introduced to detect low-power picosecond impulses and to extract the repetition rate with a low timing jitter.

Wireless synchronization of a distributed array with widely spaced sparse elements is a key enabler in coherent combining of signals in space. The angular resolution of an imaging array can be enhanced by increasing the aperture size of the array, which demands a precision synchronization link with a small timing jitter among the array elements. A wireless method for synchronizing multiple chips will ease the scalability of the array. Millimeter-wave Continuous Wave (CW) sources have been used for this purpose [19]; but in CW methods, time-varying channels in a multi-path environment add Non-Line-of-Sight (NLOS) reflections to the received signal, which results in high phase and amplitude jitters. Due to the difference in the travel time, however, LOS and NLOS signals at the receiver can be separated by transmitting ultra-short pulses
via multiple antennas and utilizing spatial modulation techniques.

The authors in [20] introduced an oscillator-less direct digital-to-impulse radiator with a repetition rate of several GHz. The ringing effects generated by the trigger signal in [20], and the reflections caused by nearby objects (such as antenna packaging and DC biasing wires), all introduce undesired zero-crossings that pose a serious challenge in extracting the repetition rate in the receiver. In this work, we present a novel mixer-based receiver with an on-chip antenna to remove the undesired ringing, detect the desired high-frequency components, and generate a reference signal that is locked to the repetition rate of the incoming pulse train. The operating frequency range of this system can potentially be much larger than narrow-band injection-locking-based CW oscillators. The presented chip can detect pulses with a repetition rate of 1 to 10 GHz.

2.2 Proposed Architecture

Ultrashort impulses, such as those reported in [20], have a broad, Gaussian-like, continuous spectrum covering the mm-wave and THz frequencies. When these impulses are generated with a fixed repetition rate, their frequency spectrum becomes a Gaussian-modulated comb. If these frequency tones are passed through a nonlinear block, self-mixing occurs and the frequency of the mixer output becomes equal to the repetition rate of the impulse train (see Figs. 2.1 and 2.2). It is important to note that due to the high-frequency contents of the impulse train, simple linear filtering cannot be used to extract the repetition rate.

The single-chip impulse receiver reported in this work consists of a broadband, on-chip, bow-tie antenna; a four-stage, narrowband, low-noise amplifier (LNA) centered at 50GHz; a nonlinear block to perform self-mixing; a low-pass filter; and a chain of baseband amplifiers. The circuit schematics are illustrated in Figs. 2.2, 2.3, and 2.4.
Figure 2.1: Example of a Gaussian pulse train in the time and frequency domains

Figure 2.2: Block diagram of the receiver and circuit schematic of the nonlinear block
Figure 2.3: Detailed circuit schematics of the input antenna and amplifier stages

The bow-tie antenna has a resonance frequency of 50 GHz (pulse center frequency). A silicon lens is used on the back of the chip to reduce the substrate modes caused by the substrate. The four-stage low-noise narrowband amplifier amplifies the received signal in the 40–60 GHz band and has a simulated peak gain of 28 dB. The amplified components are fed to an NPN-based nonlinear block. The nonlinearity of this block can be controlled by varying the bias voltage (Vb) of the base. Because the goal is to perform mixing on multiple tones of a single signal, and no high-power LO input is available, a conventional mixer (such as Gilbert cell) is not practical. In this design, the intermodulation products at the output of the mixer do not degrade the performance of the circuit because they have the desired repetition frequency or its harmonics. To reject the high-order harmonics, a fourth-order Chebyshev low-pass filter with a cutoff frequency of 10 GHz is used immediately following the mixer stage to attenuate the high-frequency components and the direct coupling from the input.

The receiver reported in this work has a tunable center frequency for extracting a wide range of pulse repetition rates ranging from 1 to 10 GHz. This is achieved by using a two-stage tunable baseband amplifier to select the desired frequency component. Each stage uses an inductor in parallel with two branches of switched varactors to control the center frequency (see Fig. 2.4). The baseband amplifier has a simulated gain of 27.5 dB when tuned at 5 GHz. The output signal is then fed to a source
follower buffer stage to drive a 50-Ω load.

Figure 2.4: Detailed circuit schematics of the baseband amplifiers and output buffer

2.3 On-chip Antenna

Receiving an ultra-short pulse with an on-chip antenna requires high efficiency in a large bandwidth due to the broadband spectrum of 8-psec pulses. A traditional dipole antenna may reach high radiation efficiency in its center frequency but it cannot be used for capturing components over a wide range of frequencies. A bow-tie antenna can potentially radiate over an infinite range of frequencies. To minimize the substrate modes, increase the radiation efficiency, and minimize the ringing, the antenna is coupled to a silicon lens through a 250-μ-thick silicon substrate. The resistivity of the silicon lens is 10KΩ.cm. The bow-tie antenna is implemented on the top metal layer of the process (LB). The length of the antenna is designed to be 0.82 mm. Simulation results show 50 GHz as the first resonance frequency of the antenna in which the imaginary part of the antenna impedance ($Z_{11}$) equals zero. A matching transmission line between two aluminum layers of LB and EA feeds the input amplifier stage from the bow-tie antenna.
2.4 Measurement Results

Two measurement setups have been used to characterize the performance of the chip. In the first setup (Fig. 2.5), two synchronized RF signal generators are used to produce two high-power frequency tones in the range of 40 to 50 GHz. These signals are then fed to horn antennas and combined in the air before arriving at the chip. The combined signal has a pulse-shaped waveform in the time-domain. Measurement results, including the output spectrum, phase noise, and timing jitter, are shown in Figs. 2.6, 2.7, 2.8, and 2.9. The output of the receiver chip indicates a root mean square (rms) timing jitter of 376 fsec. This value is compared with the 360 fsec timing jitter of the 48 GHz source in the same figure. In this measurement, the power of the synchronized sources is set at 10 dBm. The receiver is placed at a distance of 10 cm from the antennas.
Figure 2.6: Measured time-domain output waveform for 42 and 48GHz sources

Figure 2.7: Measured output spectrum for three sets of frequencies

Figure 2.8: Comparison of the measured timing jitter of the output and the source
Figure 2.9: A comparison between the measured phase noise of the 42G source and the 6GHz carrier at the output when f1=42GHz, f2=48GHz

Figure 2.10 reports the measured nonlinear behavior of the circuit, where the effect of the base voltage on the measured output power is described. In this measurement, the strongest second-order nonlinearity at an optimum base voltage of 0.87V is achieved. Fig. 2.11 shows how the measured output power of the chip varies with the source power, thus demonstrating the linear behavior of the receiver.

In the second measurement setup, shown in Fig. 2.12, an impulse-radiating chip is used to radiate a broadband ultra-short pulse train with a repetition rate of 3.1 GHz. The time-domain waveform of the radiated pulse train, measured by a customized printed circuit board (PCB) antenna and a sampling oscilloscope, is also shown in Fig. 2.12. A polyethylene lens with a focal length of 60mm is placed between the chips to increase the signal power. The total distance between the transmitter and the receiver is 10 cm. Measurement results, including the output spectrum, phase noise, and timing jitter, are shown in Figs. 2.13, Fig. 2.14, Fig. 2.15, and Fig. 2.16. Compared with the 3.1GHz reference from the signal source, the synchronized signal phase noise has not substantially deteriorated. It should be noted that at high
Figure 2.10: Measured output power of the chip vs. the base voltage of the main bipolar transistor

Figure 2.11: Measured output power of the chip vs. the power fed to a 26dB horn antenna (located at a 10-cm distance)
frequency offsets, phase noise measurement is limited by the spectrum analyzer noise floor due to the low power of the signal, so it becomes flat at -90 dBc/Hz (the actual phase noise is smaller than this value). The receiver generates a 3.1GHz reference clock with a phase noise of -89 dBc/Hz at 100-Hz frequency offset. This also includes the noise contributed by the impulse-radiating chip and the measurement error caused by the low power of the signal. In this measurement, the trigger signal that is fed to the impulse-radiating chip produces a 3.1 GHz signal with 270fs timing jitter and -89 dBc/Hz phase noise at 100 Hz offset. In the two-tone (42 and 48 GHz) test, the receiver generates a 6GHz reference clock with 376 fs timing jitter and -81 dBc/Hz phase noise at 100 Hz frequency offset. The timing jitter of the two-tone experiment is lower than the impulse-based measurement due to the higher power of the radiating source, which makes the jitter measurement more accurate and results in higher-frequency stability. The performance of the chip is compared with the prior art in Table 2.1.
Figure 2.12: Test setup for precision time transfer using a picosecond impulse radiator

Figure 2.13: Measured output spectrum of the chip
Figure 2.14: Measured output waveform of the chip (including harmonics and high-frequency couplings)

Figure 2.15: Measured timing jitter of the output waveform of the chip
Figure 2.16: Measured phase noise of 3.1GHz carrier at the output compared with the 14-dBm 3.1-GHz source

Figure 2.17: Chip micrograph of the pulse-based wireless synchronization receiver
This chapter introduced a new method for wireless time transfer using ultra-short picosecond pulses. It demonstrates the lowest timing jitter ever achieved in a wireless synchronization system. The chip includes an on-chip antenna, low-noise amplifier, a core nonlinear block, low-pass filter, and tunable baseband amplifiers. The chip is fabricated in 0.13µm SiGe BiCMOS process technology. The micrograph of the chip is shown in Fig. 2.17. To the best of the author's knowledge, this is the first receiver in silicon that can detect sub-8psec electromagnetic pulses.
Chapter 3

An Instantaneous Frequency-to-Voltage Converter

3.1 Introduction

In chapter 2, I presented a novel receiver for detecting the repetition rate of an arbitrary ultra-short impulse train. Detecting the repetition rate enables us to generate synchronized clocks in multiple chips so that they can run concurrently as separate elements of a large array. The detected clock can also be used to run a sampling system to sample the pulse train to detect the exact waveform. In this chapter, the goal is to solve a similar problem for continuous-wave (CW) systems. We would like to build a receiver that can detect the frequency of an arbitrary CW signal in order to use it for tuning the RF blocks inside the system based on the signal that we receive.

Advances in wireless communication systems and rapid occupation of various radio-frequency bands have created a need for smart reconfigurable systems and sensors that can detect the operating frequency of the received electromagnetic waves. A significant amount of work has been done in recent years to develop cognitive radio systems that can sense used RF channels in the environment and allocate unused frequency bands for their operation. A frequency-detector circuit is a key enabler for the front-end of such systems that can be used to build frequency-locked loops, as
well as self-tuned reconfigurable receivers. The output settling time in such circuits needs to be short so that fast spectrum sensing can be achieved for the purpose of frequency-hopping.

In this work, I have designed and implemented a high-speed frequency-to-voltage converter (FVC) that can detect the instantaneous frequency of the input signal with a 2.6 GHz bandwidth. This circuit can be used in cognitive radio systems to fulfill the need for sensing used frequency channels. It is also an essential block in frequency-locked loops [25]. The proposed frequency detector is based on the idea of detecting consecutive rising edges of the incoming signals to make the detection faster. [25, 26] have presented methods based on charging one capacitor and discharging it to another capacitor using two or three switches. However, this architecture requires several cycles to converge the output voltage to the final DC value, thus causing a large settling time and limiting the frequency-locked loop performance. In contrast, the architecture in the present work, the proposed architecture can generate its final output in one cycle of the input, i.e., 1-ns for a 1-GHz input. Implementing the architectures in [25, 26] also requires several control signals to adjust timings, which are eliminated in this work. Two other studies [27, 28] have also presented a frequency-to-current converter capable of tuning a voltage-controlled oscillator (VCO), but they cannot achieve high-enough frequency for many wireless applications.

### 3.2 Circuit Architecture

In this section, the architecture of the proposed high-speed frequency-to-voltage converter is presented. In order to avoid the effect of analog input amplitude on the output voltage, we apply the input signal to a high-gain amplifier to saturate it and then utilize a digital method to measure the frequency. This method is based on detecting the consecutive rising edges of a signal and charging a capacitor during...
this time interval so that the final voltage of the capacitor will be proportional to one period of the input signal. [25, 26] have used accumulating methods, which take several cycles to produce the desired output and thus have large settling times. In the proposed method, in contrast, the instantaneous frequency is measured after one cycle, which is the fastest possible settling time. The circuit has a certain operating bandwidth (2.6 GHz), but the frequency range can be extended by adding a mixer and shifting the center frequency.

The overall architecture of the proposed architecture is illustrated in Fig. 3.1. After introducing a high gain to the sinusoidal input, a sharp square-wave signal is generated. The generated square-wave signal passes through two positive edge detectors, which detect the first and second rising edges of the signal. The system has a reset input, which starts the frequency measurement. The second edge detector has an enable input, which is generated after the first edge detector detects the first rising edge. The output capacitor is connected to a current source and can only be charged when both of the PMOS switches (M1 and M2) are on. Because the charging happens only between the first two rising edges of the input, the final output voltage becomes proportional to one period of the signal. After this step, the output voltage remains constant until the reset input resets the operation of the system.
Figure 3.2: Detailed circuit schematics of the first stage of the FVC

Figure 3.3: Detailed circuit schematics of the first and second edge detectors
Figure 3.4: Detailed circuit schematics of the output capacitor charging mechanism and the output buffer

A detailed circuit schematic diagram of the proposed FVC is illustrated in Figs. 3.2, 3.3, and 3.4. The edge-detector circuits may conventionally be implemented using digital latches and flip-flops but they do not provide enough speed and they consume high power. In the proposed edge-detector circuits, only three transistors are employed, using a feedback topology. The output voltage of this block will be saturated when a transition from 0V to 1V occurs in the input signal. The second edge detector has a larger delay time on its path to make sure that it does not detect the first rising edge of the signal. A NAND gate directly between the delay line and the second edge-detector generates a pulse with the same frequency but a smaller duty cycle than the input signal. This block is used to limit the operation of the second edge detector to a much shorter time so that its output does not saturate during the rest of the first cycle. A brief timing diagram describing the transitions of each node voltage is shown in Fig. 3.5.

A voltage buffer is used after the output node to drive the 50-Ω input impedance
of the oscilloscope. This buffer consists of two stages of source followers. The PMOS source follower increases the level of the output by a certain amount, which is then cancelled by the NMOS source follower with the same level shift. Thus, the output voltage level will not change from its expected value, while it can drive the 50-Ω load.

### 3.3 Measurement Results

The fabricated frequency-to-voltage converter is characterized using a sampling oscilloscope (Agilent DCA-X 86100D) and SMA cables/connectors. A block diagram of the test setup is illustrated in Fig. 3.6. An RF signal generator (HP 8340B) and a low-frequency arbitrary waveform generator (AWG; Agilent 33250A), the latter of which is used for generating the reset signal, are synchronized using a 10-MHz reference signal.
A 10-MHz reset signal is generated with the AWG to reset the operation of the circuit every 100 ns. Applying a 1-GHz signal to the circuit input will result in an output voltage converging to 240 mV, as shown in Fig. 3.7. The transition phase of the output voltage is also shown in Fig. 3.8, which demonstrates a charging time equal to one input cycle, i.e., 1 ns at 1 GHz. The output voltage resulting from a 2.6-GHz input is also shown in Fig. 3.9.

Fig. 3.10 illustrates how the output voltage changes by increasing the input signal frequency. The strong correlation between these two parameters proves that the output voltage of the circuit can be used to calculate the signal frequency. Table 3.1 compares this work with the prior art.

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<td>Maximum Input Frequency</td>
<td>2.6 GHz</td>
<td>5 GHz</td>
<td>1.15 GHz</td>
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<tr>
<td>Settling Time</td>
<td>1 ns at 1 GHz (one cycle)</td>
<td>100 ns at 83.3 MHz</td>
<td>500 ps at 1.15 GHz</td>
</tr>
<tr>
<td>Minimum Input Power</td>
<td>-17.7 dBm @ 1 GHz</td>
<td>N/A</td>
<td>N/A</td>
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<td>Chip Area</td>
<td>0.132 mm$^2$ (with pads)</td>
<td>0.22 mm$^2$ (FLL)</td>
<td>0.015 mm$^2$ (estimated, with VCO)</td>
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<td>90nm CMOS</td>
<td>350nm CMOS</td>
<td>180nm CMOS</td>
</tr>
</tbody>
</table>

Table 3.1: Comparison of the presented FVC with prior art.
Figure 3.7: Measured time-domain output waveform for a 1-GHz input and a 10-MHz reset signal with a 500-ns timespan

Figure 3.8: Measured time-domain output waveform for a 1-GHz input and a 10-MHz reset signal with a 20-ns timespan
Figure 3.9: Measured time-domain output waveform for a 2.6-GHz input

Figure 3.10: Measured output voltage versus the sinusoidal input frequency
3.4 Conclusions

In this chapter, a frequency-to-voltage converter with a single-cycle settling time is reported. It employs two novel edge detector blocks, several digital gates, and a buffer that drives a 50-Ω load. The converter operates with an input frequency range of up to 2.6 GHz, while consuming 6.5 mW from a 1-V power supply. The output voltage changes from 440 mV to 45 mV by varying the input frequency from 200 MHz to 2.6 GHz. This work is fabricated in a 90nm CMOS process technology. The size of the chip, including the pads, is 440 µm × 300 µm. A micrograph of the chip is shown in Fig. 3.11.
In this dissertation, two different integrated circuits are designed, fabricated, and tested to operate in the RF/mm-wave frequency regions. A mm-wave impulse receiver is introduced that is capable of detecting ultra-shot picosecond pulses and synchronizing multiple chips with a sub-ps precision. An RF frequency detector is also discussed for detecting the frequency tone of the received signal.

The proposed impulse receiver in chapter 2 is based on the novel idea of self-mixing among the frequency tones of a single repetitive impulse train. The fabricated chip is capable of detecting sub-10psec pulse trains and locking a generated clock to the repetition rate of the pulse train, which varies from 1 to 10 GHz.

Chapter 3 discussed a new method for building instantaneous frequency-to-voltage converters that relied on detecting the first two rising edges of the received signal. This new architecture was fabricated in a CMOS process technology; measurements demonstrated an operating frequency of up to 2.6 GHz. The advantage of this circuit block over the prior work is the fast conversion time, which can detect the input frequency after two input cycles.

The work in chapter 2 was presented and published in the IEEE International Microwave Symposium 2016 [29], while the work in chapter 3 was presented and pub-

In conclusion, this dissertation presented novel circuits and systems that can be utilized in building broadband RF/mm-wave receivers.


[23] X. Yang, X. Lu, and A. Babakhani, “Picosecond wireless synchronization using an optically locked voltage controlled oscillator (OL-VCO),” IEEE MTT-S Int. Microwave Symp. Dig., 2014. 2.4


[29] B. Jamali and A. Babakhani, “Sub-picosecond Wireless Synchronization Based on a Millimeter-Wave Impulse Receiver with an On-chip Antenna in 0.13m SiGe BiCMOS,” IEEE MTT-S Int. Microwave Symp. Dig., 2016. 4