RICE UNIVERSITY

OPERATION TIME MONITOR FOR A DIGITAL COMPUTER

by

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Abstract

This paper is devoted to a detailed description of a device, an operation time monitor, which is used to investigate the behavoir of the operation time in a digital computer. The principle employed to design the monitor is a very basic relation in fundamental electricity -- the voltage across a capacitor is linearly proportional to the time during which a constant charging current is flowing through the capacitor. The constant current source which provides the required charging current is controlled by the pulses conveying the input information from a digital computer. Some data obtained by this monitor are included at the end of this paper to illustrate its application to a digital computer.

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(I) Acknowledgements

A most sincere thank you should be extended to my adviser, Dr. Martin Graham, for his helpful enlightenment and continuous encouragement. The author also wishes to express his gratitude to Mr. Walter Orvedahl and Dr. Sigsby Rusk for their kind help.

(II) Introduction

While a computer is operating, arithmetic operations, logical operations, memory fetches, memory stores, and control counter advancements occupy a part of the total elapsed time. It is of interest to know the ratio of the actual ON time of each operation to the total elapsed time of a program segment (excluding the punching and printing time) and to know the average time required to execute such operations. With this information one can determine how an improvement of certain parts of a computer will affect the efficiency of the whole computer. For instance, if the time required to get control of memory in a memory fetch operation is large and if its ratio with respect to the total memory fetch time is also large, then it is worth considering improving the memory mechanism on the basis of overall time-efficiency and cost.

The purpose of this paper is to propose methods and a circuit design to accomplish the time measurements on any operation of interest. It should be pointed out that the computer is assumed to be able to supply pulse signals when the operations under investigation start and when they stop.

Two approaches were considered and one of them has been adopted. An operation time monitor, based on the adopted approach, has been built for the Rice Computer. These two approaches are described briefly in the following:

(A) In Figure 1, a fixed-frequency reference signal coming from an oscillator and the information of START and STOP signals coming from the computer after a flip-flop are sent to an AND gate. The output of the AND gate is fed into an electronic counter. The counter reading and a conventional watch or clock give the total operation ON time and the total elapsed time respectively.

This method has the following problems. Higher frequency reference signals can give more accurate time readings but a more expensive counter is required and troublesome stray effects associated with high frequencies are present. On the other hand, lower frequency reference signals avoid the troubles mentioned above but unfortunately at the sacrifice of time accuracy which is important. Hence this method was not used.

(B) The second approach, adopted here, is shown in Figure 2. The SWITCHING UNIT, actuated by a flip-flop whose state is determined by the START and STOP signals, controls S1 which, in turn, gates a constant charging current to capacitor C. When the voltage across C reaches a preset value, the DISCHARGING UNIT closes S2 which discharges C. Meanwhile, the counter, triggered by the discharging pulse, is increased by one. The following equation

$$i.\Delta t=c.\Delta V, \text{ or } \Delta t=c.\Delta V/i$$

gives the time, Δt, between two consecutive discharging pulses.

Therefore, the total ON time of the input flip-flop can be determined from the reading of the counter and the residual voltage across the capacitor C. A clock or watch is needed to obtain the reference total elapsed time.

Since less expensive components can be used to build a device based on the second method, the rest of this paper is devoted to describing the circuit design, operation, and application of the device based on the second method.

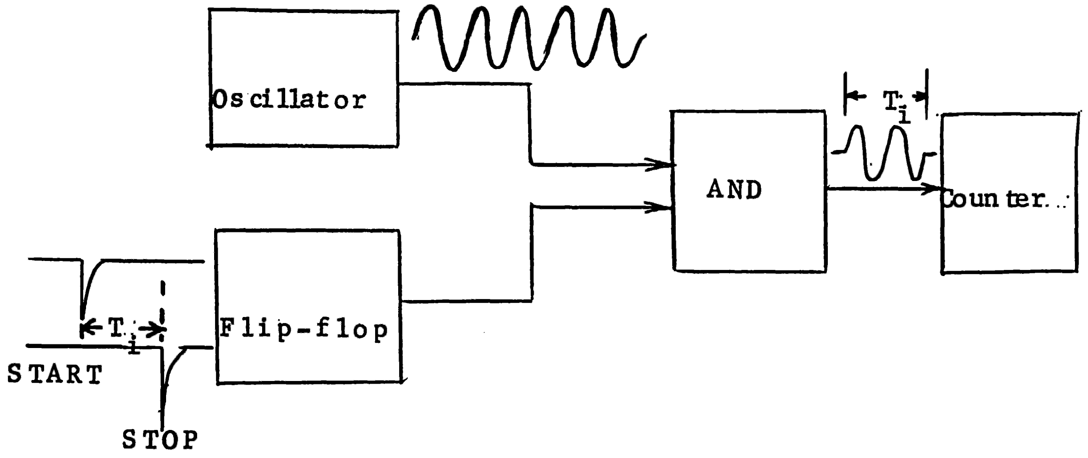


Figure 1.

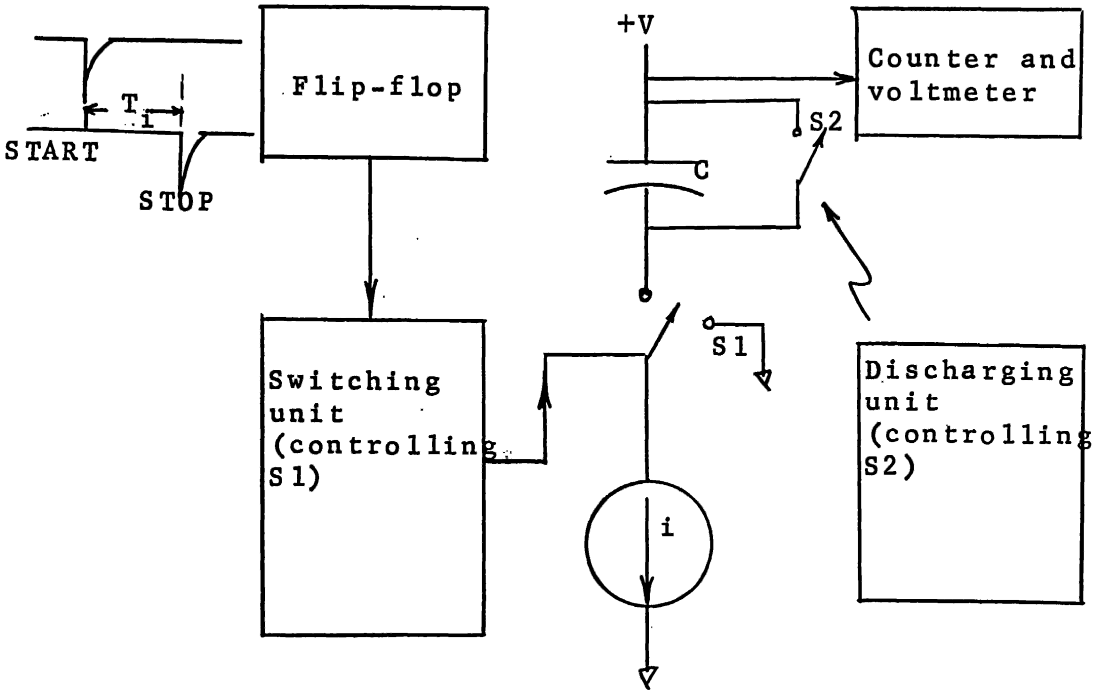


Figure 2.

(III) Circuit Design

(A) A General Description

While the computer is running, the START and STOP signals coming from the parts of the computer which are of interest have the configuration shown in Figure 4. The actual waveform of individual pulses in the Rice Computer are shown in Figure 5.

The first thing we want to know is the total ON time, namely, $T_k+T_{k+1}+$ ---- $+T_{k+j}$, during the whole reference time T_t. The second thing is the number of START signals during T_t.

When the total ON time is needed, the START and STOP signals should be sent to the input flip-flop (Figure 3.). During the period after a certain START signal and before the associated STOP signal, the output of the flip-flop through the current switching stage closes switch S1 and lets the capacitor C be charged by constant current i. Meanwhile, the voltage across the capacitor, V_c, linearly increases with time. After the STOP signal and before the next START signal, S1 is open. When V_c reaches a preset value V_{co} after a period of ON time, Δt, the discharging mechanism discharges C and sends out a pulse. Therefore, it is obvious that the number of such pulses, I, and the residual voltage across the capacitor reveal the total ON time during the whole investigating period. The pulses are fed into a univibrator which drives an electromechanical counter in order to register the information conveyed by the pulses. Simultaneously, the pulses are also fed into another univibrator which drives a relay. This relay is used to short C for a very fast discharging of C; in other words, to decrease the percentage error introduced by the time required to discharge C.

When the number of START signals during T_t is sought, the START signal is sent to the input univibrator as shown

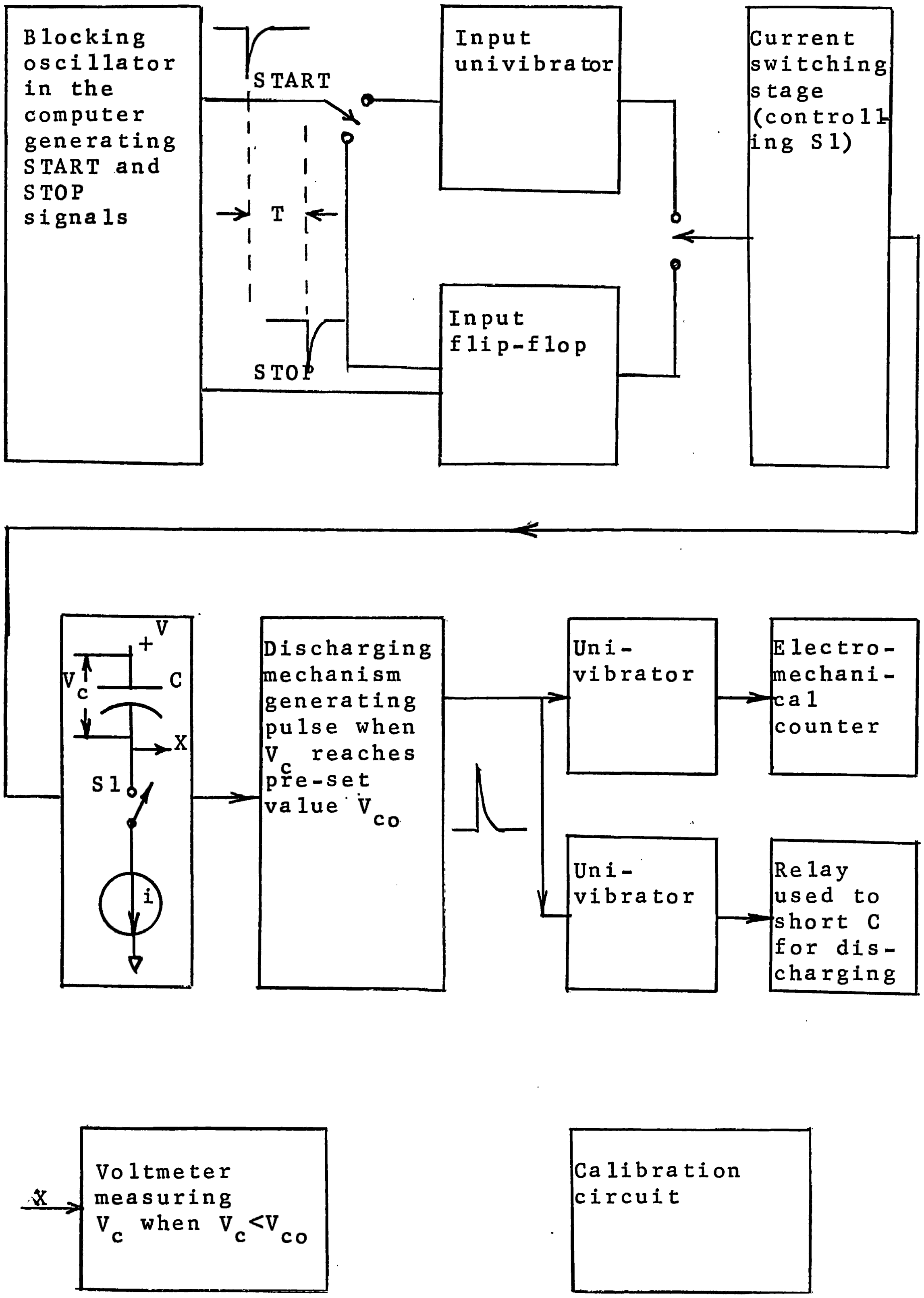

Blocking oscillator in the computer generating START and STOP signals
START
T
STOP
Input univibrator
Input flip-flop
Current switching stage (controlling S1)
V
+
V_c
C
X
S1
i
Discharging mechanism generating pulse when V_c reaches pre-set value V_{co}
Uni-vibrator
Electro-mechanical counter
Uni-vibrator
Relay used to short C for dis-charging
X
Voltmeter measuring V_c when $V_c<V_{co}$
Calibration circuit

Figure 3.

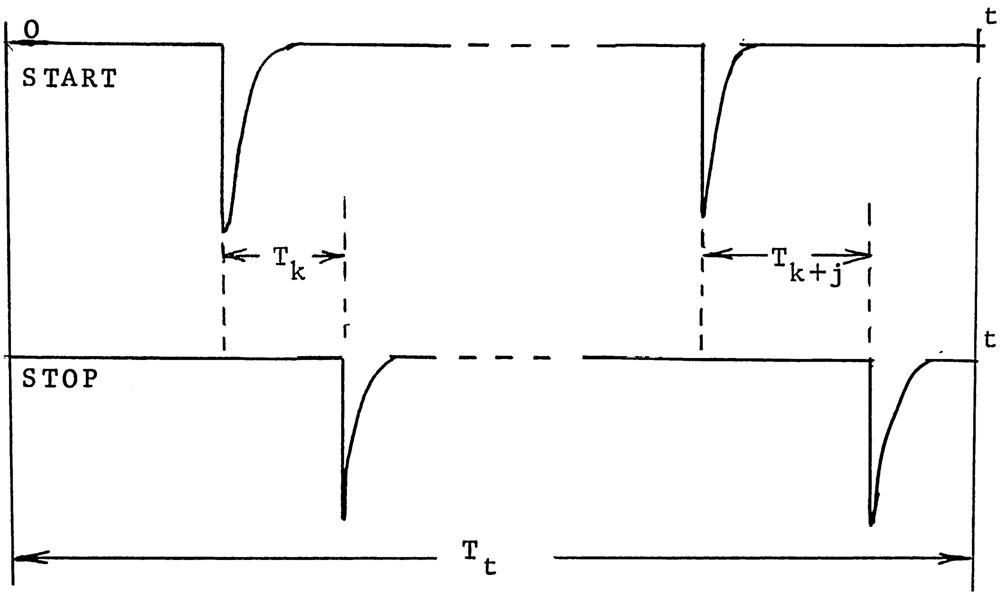


Figure 4.

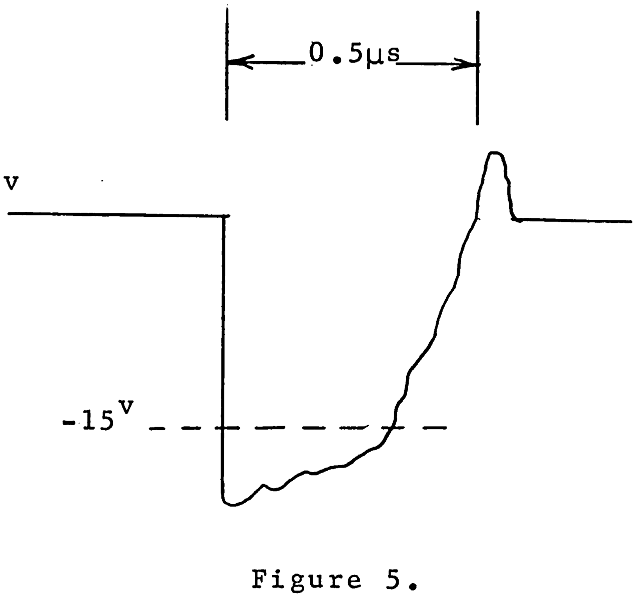


Figure 5.

in Figure 3., instead of the flip-flop. In response to each input START signal, the univibrator generates an output pulse of fixed width t_o which is used to gate the following current switching stage. Therefore, the final total ON time reading divided by the fixed width t_o should be the number of START signals during T_t.

At the end of the whole investigating period, the voltage across the capacitor, $V_c<V_{co}$, should be read because it bears the information of fractions of Δt. Hence a voltmeter is needed. This voltmeter must have a very high input impedance in order not to influence the capacitor.

In addition, a calibration circuit has been designed for the purpose of maintaining the accuracy of the device.

(B) Individual Component Design

1. Input Flip-flop

The function of the input flip-flop is to switch between two specified states in response to the START and STOP signals for the purpose of gating the following current switching stage. The circuit diagram is shown in Figure 6. The input signal waveform presented to the input flip-flop and the output waveform it is required to generate are shown in Figure 7.

Let us designate the transistors in the flip-flop "1" and "2" respectively. Assume "1" off, "2" on:

$e_{c2}=0^v$, or practically around -0.2^v

$e_{b2}=0^v$, or practically around -0.3^v

$e_{e2}=0^v$

$e_{c1}=-10^v$

$e_{b1}=10-(10/(3+6.8))6.8=3^v$

$e_{e1}=0^v$

Whenever the negative START signal comes in, the off transistor, "1", is turned on and the on

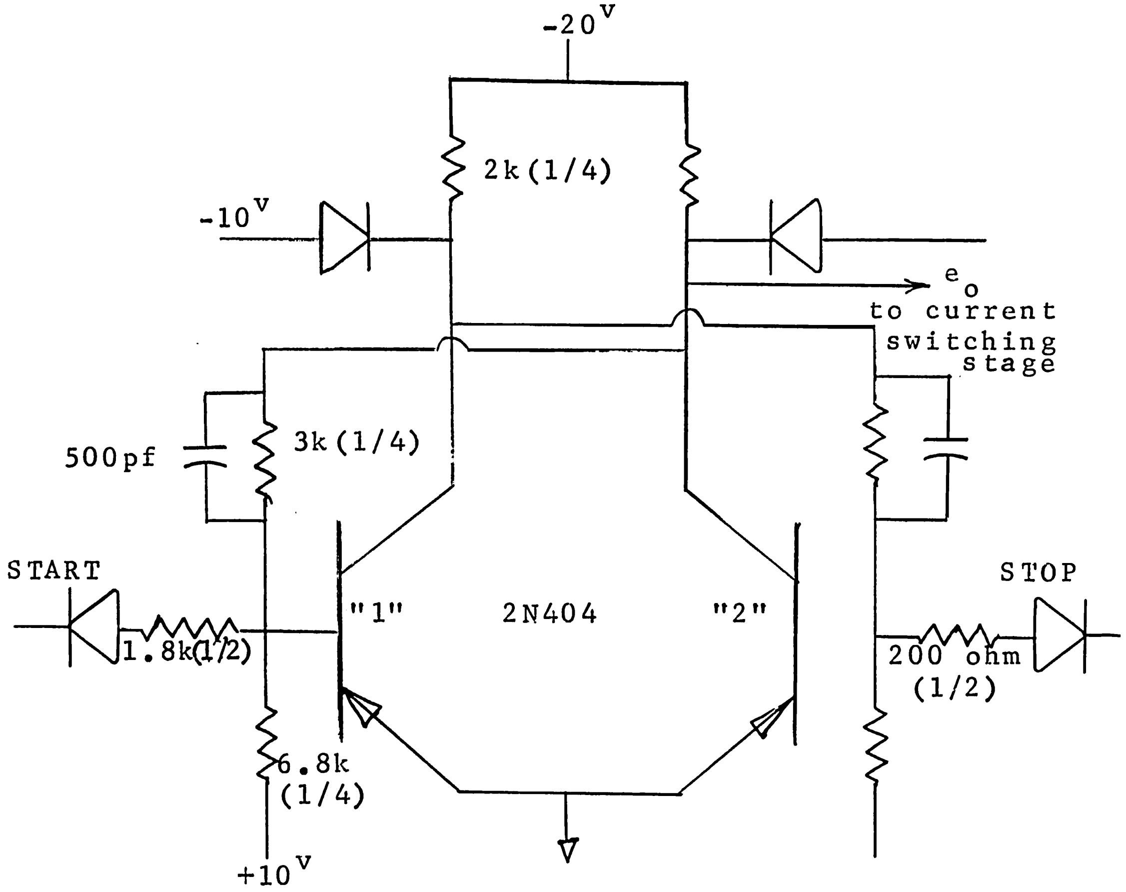


Figure 6.

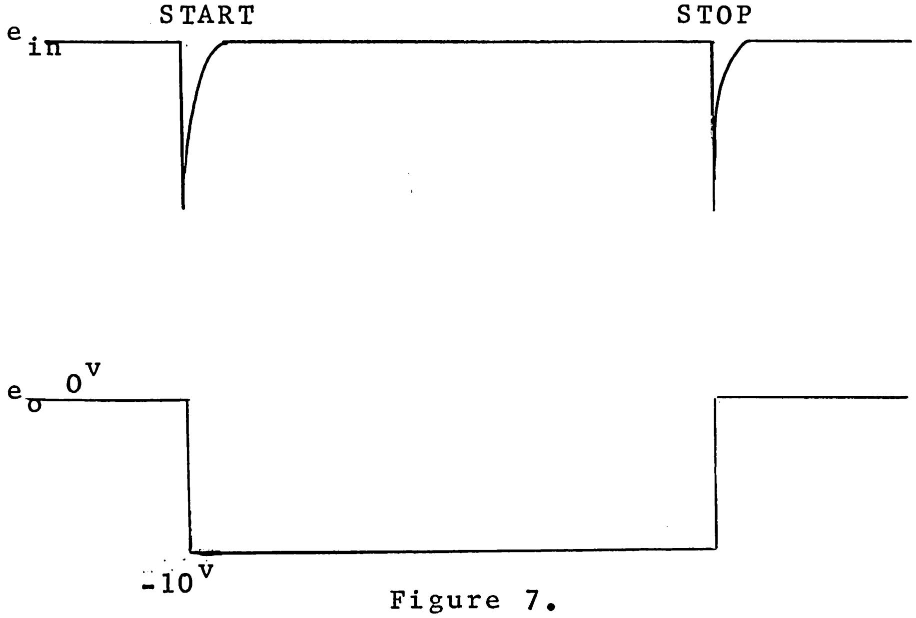


Figure 7.

transistor, "2", turns off. Later on, the STOP signal comes in, the states of "1" and "2" are interchanged. Since e_{c2} is taken as the output of the flip-flop, we see that it performs just in the way required in Figure 7. PNP transistors, type 2N404, are used because the input triggers are negative pulses. Catch diodes are used in order to get reliable operation. Crossover capacitors are used to speed up the transition of the flip-flop.

Occasionally the STOP signal follows the START signal so closely that the symmetrical flip-flop can not respond to them correctly (Figure 8-a.). There are at least two ways to improve the situation. The first one is to connect a capacitor from the base on the STOP side to ground. Since the base charging time constant is increased, the STOP signal is, in effect, widened. This is shown in Figure 8-b. If t_3 is reasonably large, the STOP signal can assure that the flip-flop be turned off at the end of t_3 no matter whether it was on or not during the period of t_1+t_2. Hence no significant error would be introduced. The second method is to increase the base current-limiting resistor on the START side by roughly ten times. This is equivalent to shrinking the START signal to approximately one-tenth of its original value (Figure 8-c.). The latter method was found reliable and employed here.

2. Input Univibrator

This circuit is used when the number of START signals during a certain period is sought. The circuit diagram and the input-output relation are shown in Figure 9. The rest of the circuits

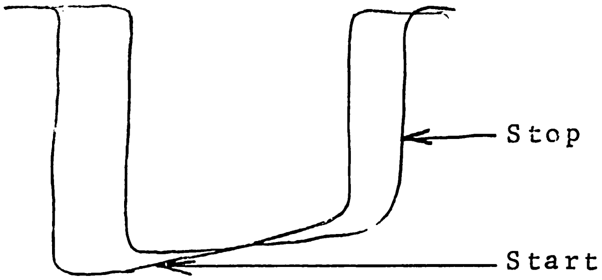


Figure 8-a.

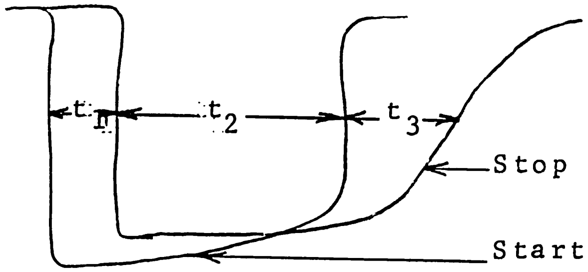


Figure 8-b.

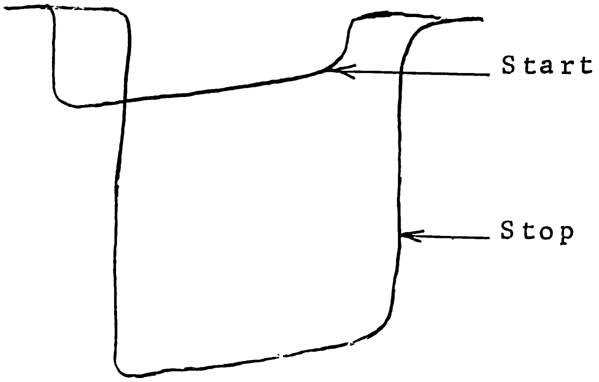


Figure 8-c.

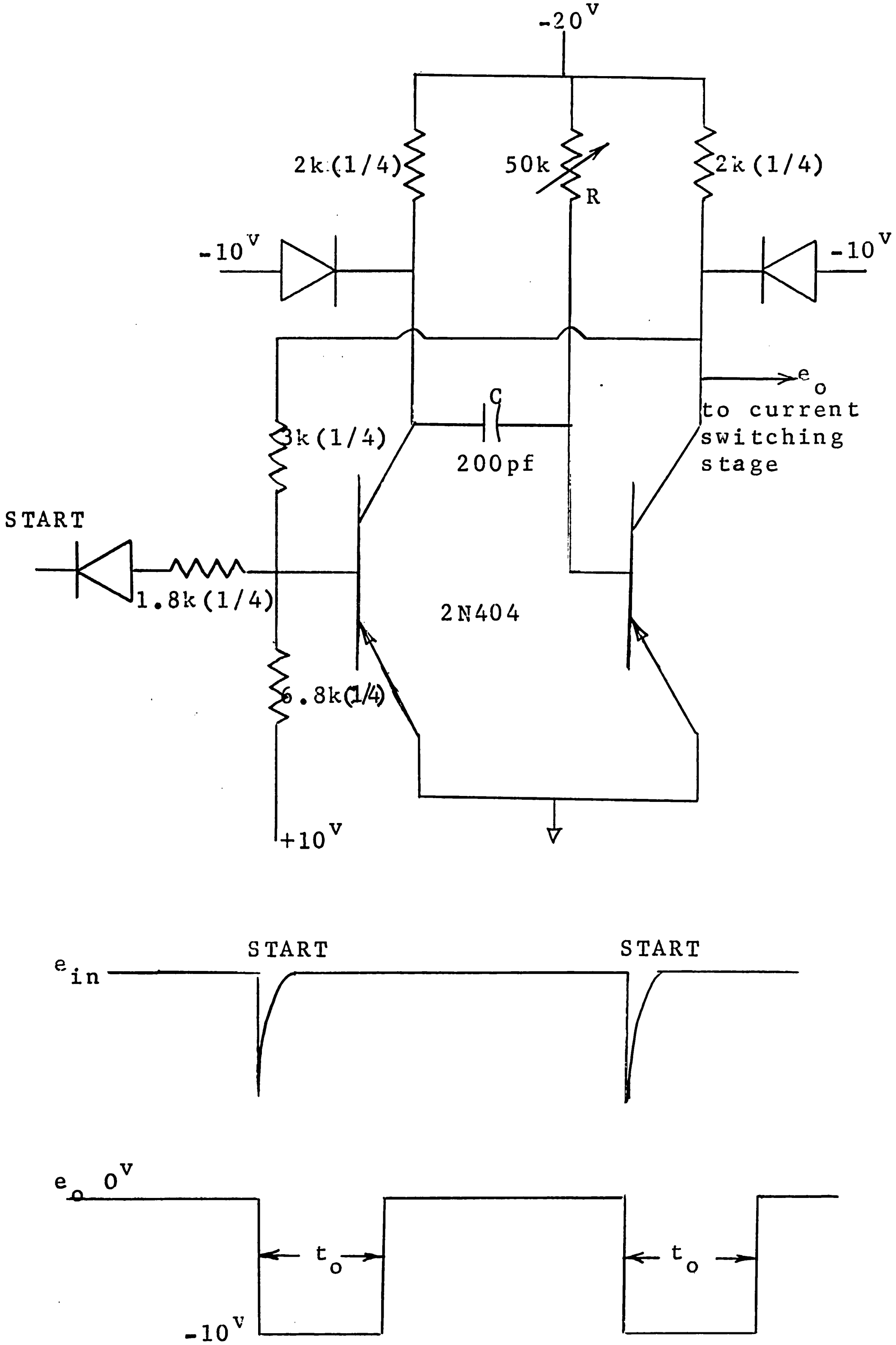

-20^v
2k(1/4)
50k
R
2k(1/4)
-10^v
-10^v
e_o
to current switching stage
C
200pf
3k(1/4)
START
1.8k(1/4)
2N404
6.8k(1/4)
+10^v
e_in
START
START
e_o 0^v
t_o
t_o
-10^v

Figure 9.

associated with this univibrator are the same as that for the input flip-flop in 1.

3. Current Switching Stage and Charging Mechanism

Referring to Figure 10., when the switch, Sa, is set at position "1", T1 is off and T2 is on. A more thorough discussion is needed (Figures 11 and 12.).

In Figure 11 which is the charging capacitor and the right section of tube 12AX7, the complete capacitor-charging current, i_c, flowing in 10meg resistor R_k, produces a proportional voltage drop which, together with the grid bias voltage, -5^V, determines the grid-to-cathode voltage; the 25k potentiometer K2 forms a variable voltage source to which the 10meg R_k is returned.

This circuit, from grid to cathode, is simply a cathode follower. Therefore, as long as the plate voltage remains sufficiently high, the grid will not draw current and we can assume unity gain as a reasonable assumption and hence the cathode voltage is roughly zero. Therefore, the charging current i_c must be

$$i_c=100^V/10\text{meg}=10\mu A$$

where the 10meg resistor R_k is assumed to return to -100^V.

Another view-point based on the Thevenin equivalent circuit can result in the diagram shown in Figure 12. In spite of the actual exponential charging toward E_{Th} with the long time constant $(\mu+1)R_kC$, the current varies very slightly over the restricted voltage range of interest. In our case, the range of interest falls between $+50^V$ and $+150^V$ which is quite small as compared with $(\mu+1)\times 100^V+150^V$ where μ is around 30.

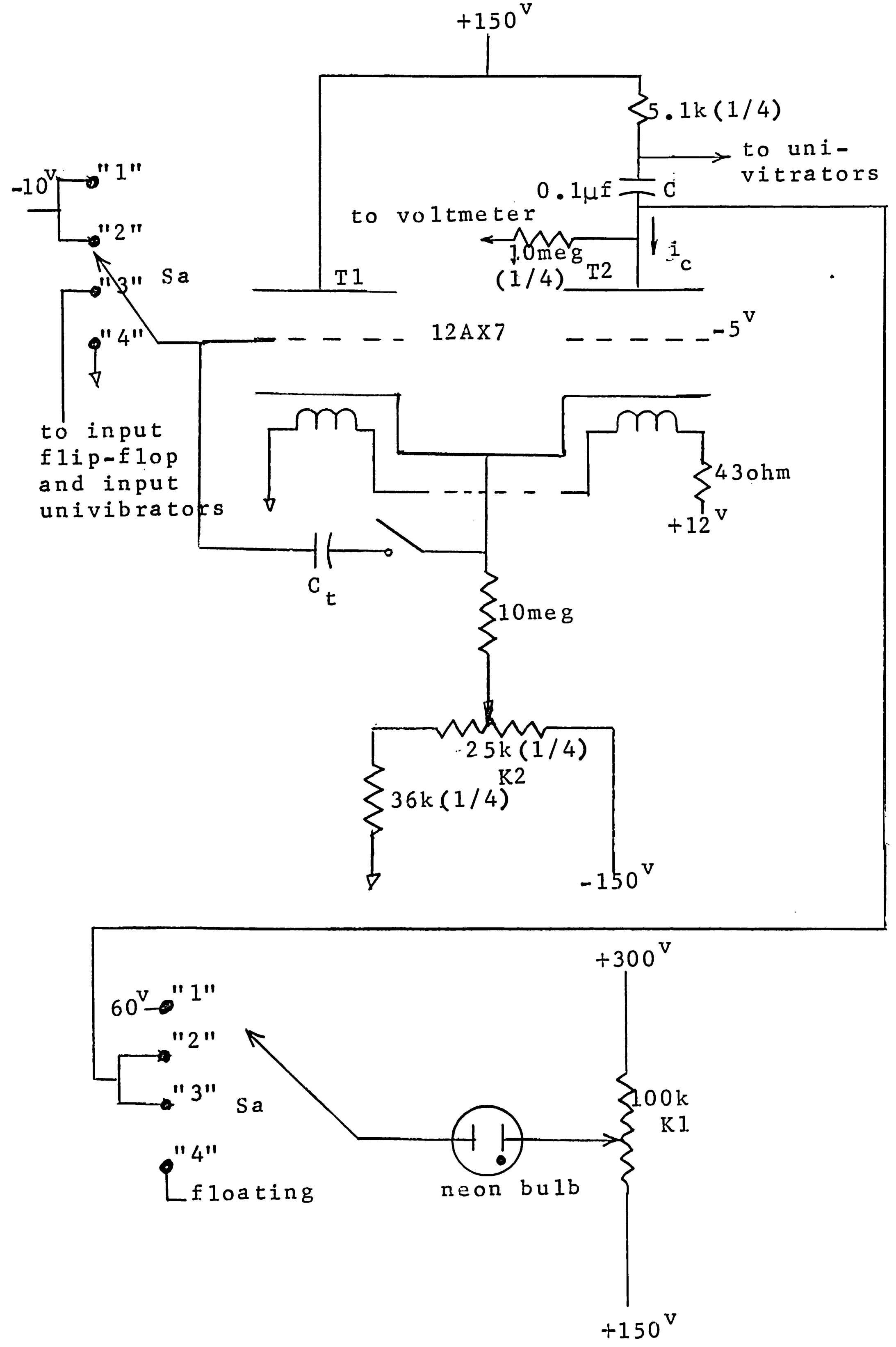

+150v
5.1k(1/4)
to uni-
vitrators
-10v
"1"
"2"
"3"
Sa
"4"
0.1μf
C
to voltmeter
10meg
(1/4)
ic
T1
T2
12AX7
-5v
to input
flip-flop
and input
univibrators
43ohm
+12v
Ct
10meg
25k(1/4)
K2
36k(1/4)
-150v
+300v
60v
"1"
"2"
"3"
Sa
"4"
floating
100k
K1
neon bulb
+150v

Figure 10.

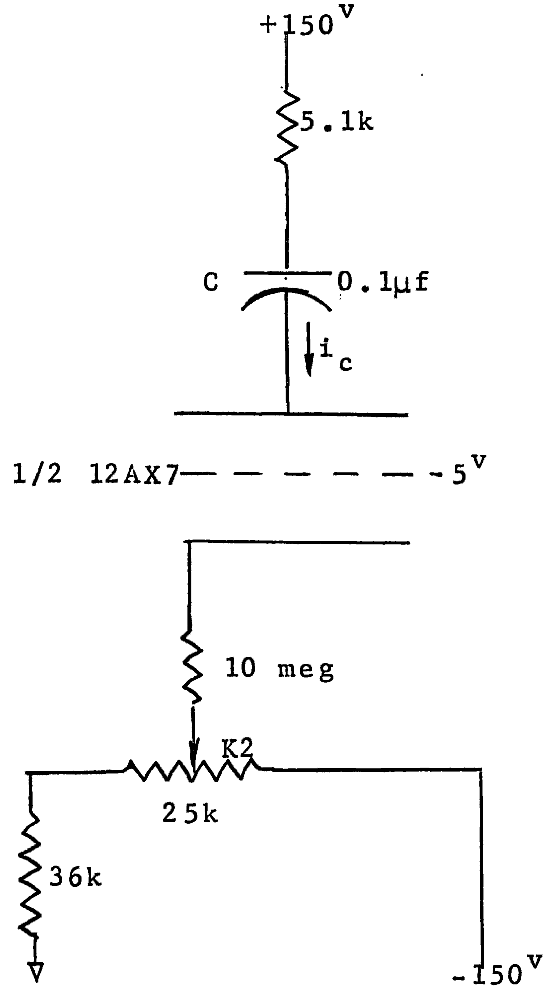


Figure 11.

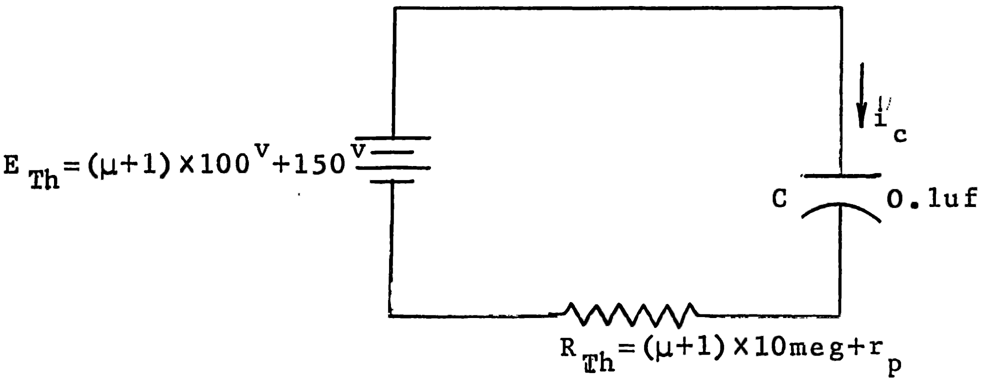


Figure 12.

In order to increase E_{Th} for the sake of better linearity in the charging curve, it is obviously very natural to employ high-μ tubes, and this is why a 12AX7 was used here. From this discussion, it is obvious that the object of obtaining a rather steady charging current has been achieved.

Since it is impossible to have all components perfectly accurate, it is necessary to have a certain amount of adjustable variation for each factor. Here, for the charging current, R_k is returned to a variable negative power supply. The variation in the power supply and that in the charging current can be seen in the following calculation:

$$|V|_{min}=150\times 36/(36+25)=88.5^V$$

$$|V|_{max}=150^V$$

Since the voltage difference between the grid and the cathode is relatively small as compared with 100^V or so and also the grid is biased at -5^V, it is reasonable to assume the cathode voltage zero in the following approximation of i_c.

$$i_{c\ min}=88.5^V/10\ \text{meg}=8.85\mu A$$

$$i_{c\ max}=150^V/10\ \text{meg}=15\mu A$$

Due to the inevitable variation in components and power supplies and also the fact that the cathode voltage is not exactly zero, the charging current can not be expected to vary ideally between the two extreme values shown above. Nevertheless, we are given the freedom to adjust the charging current to the extent required which is a vital feature in determining the behavior of the whole device.

A remark should be made here to explain why a small charging current, nominally 10μA, is employed here. From the basic voltage-charge relation we obtain

$$\Delta t = C \cdot \Delta v / i_c$$

Δt is required to be one second and Δv one hundred volts, hence it is apparent that small i_c gives the freedom to choose a small capacitor which is relatively cheaper and, in turn, this freedom is quite important and surely necessary in practical design.

Unfortunately, there are several sources of leakage current which become important in the case where a small charging current is used. The leakage charging current, or leakage plate current, can be measured, but the explanation of how to measure it is deferred to the section describing the high input impedance cathode-follower voltmeter.

It was found that the leakage current depended on both the filament voltage and the plate voltage. Since a reasonably large plate swing is needed, adjusting the filament voltage to minimize the leakage current turns out to be the only practical choice. It should be noted that this leakage phenomenon is different among tubes from different manufacturers and even somewhat different among tubes of the same manufacturers. However, the general behavior -- the leakage plate current decreases as the filament voltage decreases with grid bias and plate voltage fixed -- is common to all tubes.

Although lower filament voltage gives less plate leakage current, the fact that the filament voltage can not be so low as not to provide enough current when the tube is on should be taken into consideration. Due to this restriction, the filament voltage was chosen from experiment as 8^V. Under this condition, the leakage plate current is about 10^4 to 10^5 times less than the charging current of 10μA, yet sufficient plate current is available when the tube is on. This is satisfactory. A resistor of 43 ohms, determined by experiment, was put in series with the filament to reduce the actual filament voltage to about 8^V.

Another experimental result which should be mentioned is that when the left grid is biased at ground and the right one is biased at negative values, the magnitude of current leakage does not change appreciably until the right grid bias is increased from -10^V (or even more negative) to about -3^V.

4. Discharging Mechanism

Part of Figure 10 is redrawn in Figure 13 to explain the discharging mechanism. A slight modification, the addition of switch S_r, should be noted. Since the charging current is small, the voltage drop across the 5.1k plate resistor is negligible. In other words, $V_{"a"}$ is essentially 150^V. $V_{"c"}$ is a function of the setting of K1. The firing voltage of the neon bulb is roughly 110^V and the sustaining voltage is about 80^V or so, hence an equivalent pulse generator of about 20 or 30 volts is obtained when the neon bulb fires. As the charging current flows, $V_{"b"}$ decreases. The neon bulb fires when the difference between $V_{"c"}$ and $V_{"b"}$ reaches the firing voltage of the neon bulb. Then we obtain the equivalent circuit shown in Figure 14. In Figure 15., 0.5k is the equivalent input impedance of the two univibrators triggered by

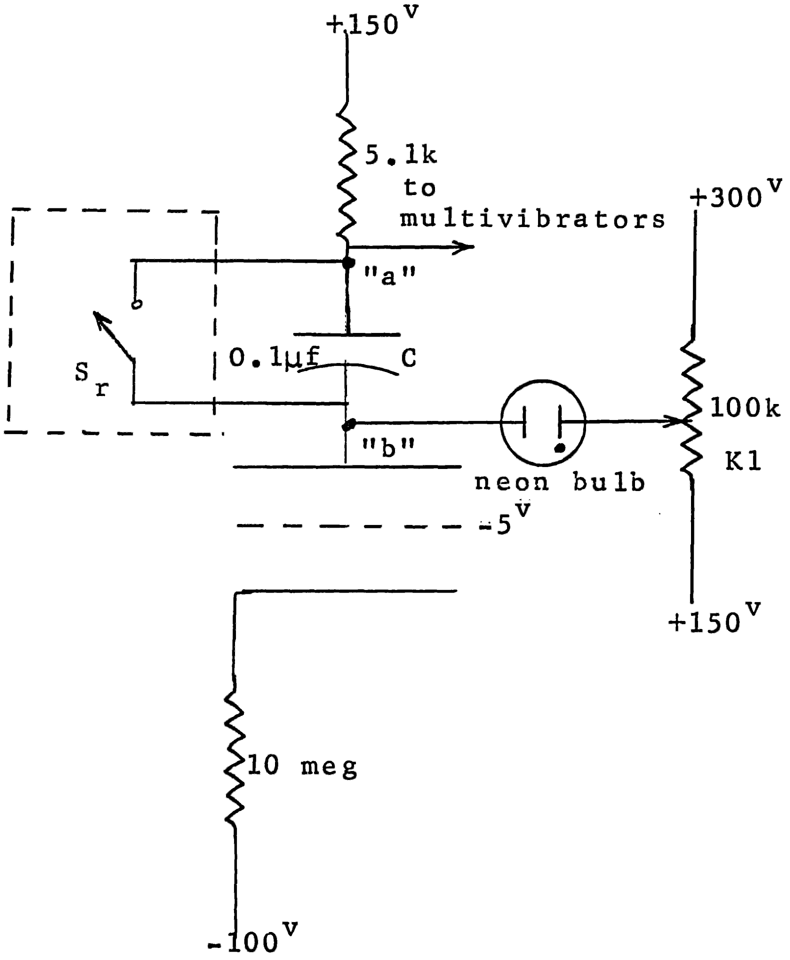


Figure 13.

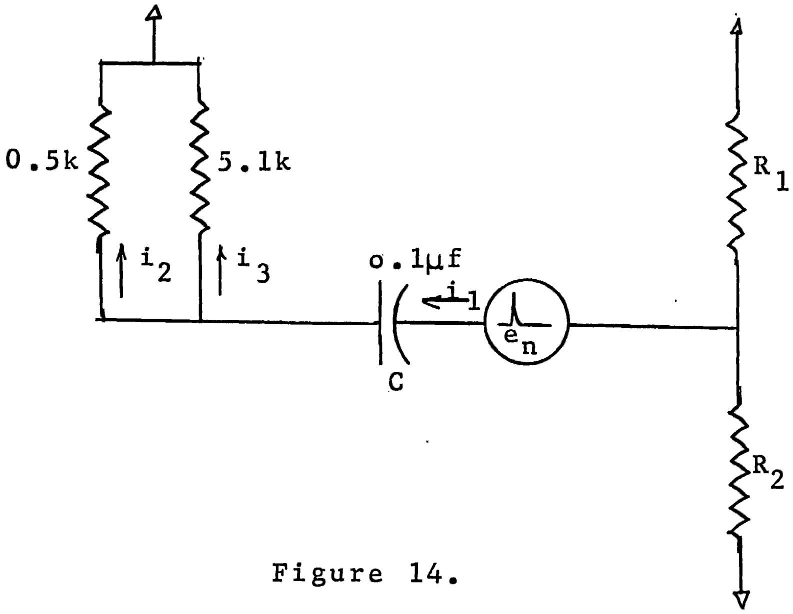
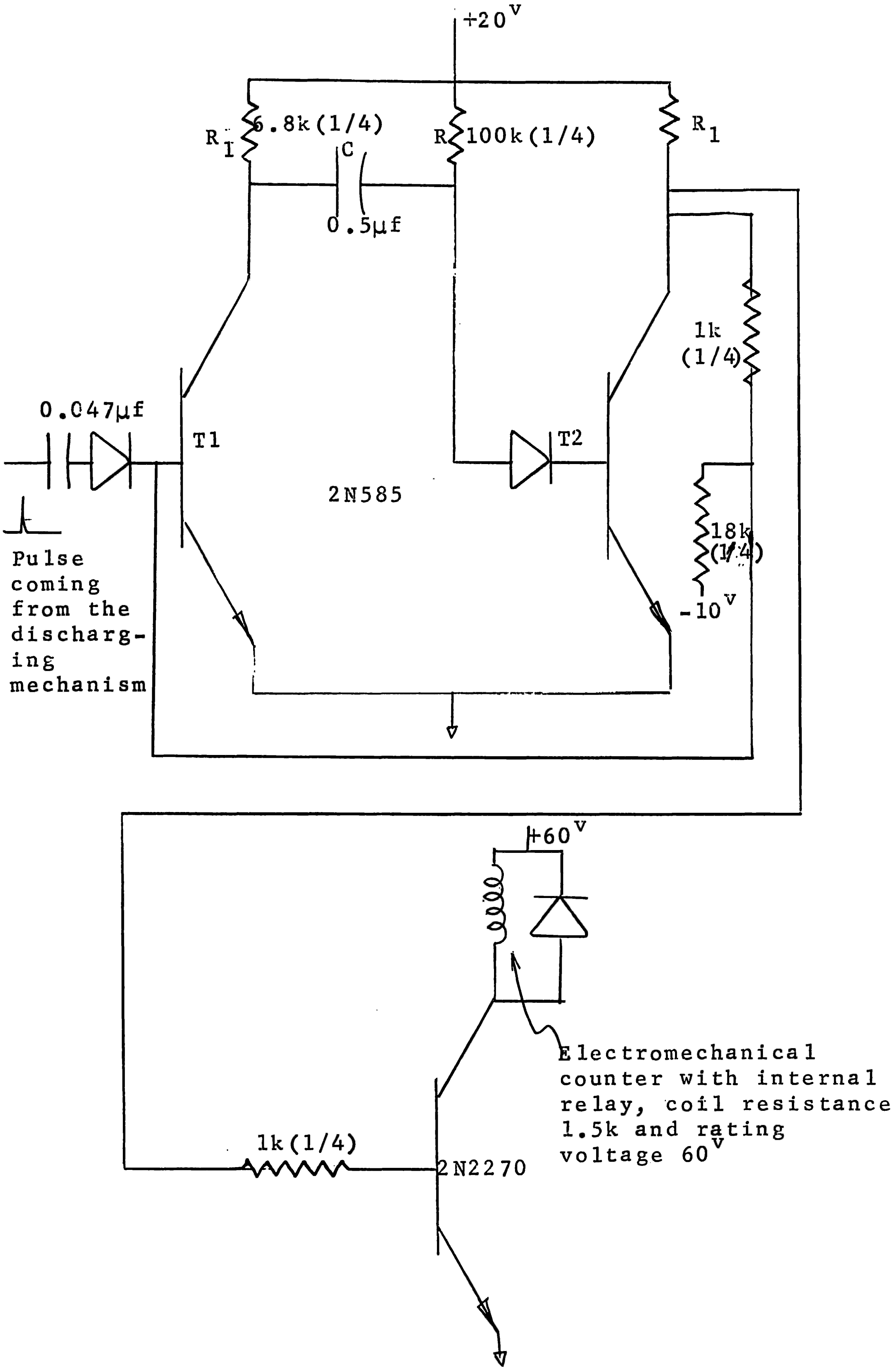


Figure 14.

the pulse generated here. This pulse is transmitted through C to the plate resistor and the univibrators. The current i_1 is primarily determined by the 0.5k resistance and the equivalent resistance of R_1 in parallel with R_2 (the sum of R_1 and R_2 is the total resistance of K1). The current i_2 is essentially equal to i_1. Because i_2 is required to be large enough to drive the two univibrators, the equivalent resistance of R_1 in parallel with R_2 should be as small as possible. One of the univibrators triggered by the pulse energizes an associated relay which, in turn, shorts C to obtain a complete discharge. This is shown schematically as the switch S_r in the dotted-line box in Figure 13 and will be discussed in 6.

5. Univibrator and the Associated Electromechanical Counter

This stage (Figure 15.) serves to receive the pulse coming from the discharging mechanism described in 4 and shape it and finally register it in the associated electromechanical counter. In the design, attention was paid to these requirements: first, the univibrator must be able to respond to the input pulse reliably; second, the output of the univibrator must be long enough to drive the associated counter yet be relatively short as compared with one second which was chosen for the device as the rate of pulse generation in the charging and discharging mechanism. The first requirement can be met by increasing the pulse current (discussed previously) and appropriately choosing resistors for the input side. For the second requirement, we should first know the time the



Pulse coming from the discharging mechanism

Electromechanical counter with internal relay, coil resistance 1.5k and rating voltage 60V

Figure 15.

counter requires to be energized. This is about twenty miliseconds for the counter used here. The width of the output of the univibrator is

$$RC \ln 2 = 0.7RC$$

or

$$(0.7)(100K)(0.5\mu f) = 35ms$$

Apparently, 35ms is long enough to make the counter work while the 2N2270 transistor is on. The diode associated with the counter is used for protecting the transistor 2N2270 from inductive transients; the diodes associated with the univibrator are used for preventing triggering by spurious pulses.

6. Univibrator and the Associated Relay

Examining the circuit diagram shown in Figure 16 reveals that this stage is almost the same as the previous one except a 0.1μf (timing capacitor) is used here instead of 0.5μf and a relay rather than the counter is to be energized.

This stage serves to receive the pulse and shape it and finally operate the relay which in turn shorts the charging capacitor C. The purpose of shorting C is to reset the plate voltage of the charging tube from its minimum value to its top value. Since we want the plate voltage to jump back as soon as possible when it reaches the minimum value, this requires the output pulse width of the univibrator to be as narrow as possible. Yet, it must still be wide enough to operate the relay, hence a compromise must be made. The error introduced by this stage should not be more than one percent; in other words, the output pulse width should be less than ten miliseconds. The relay used here has

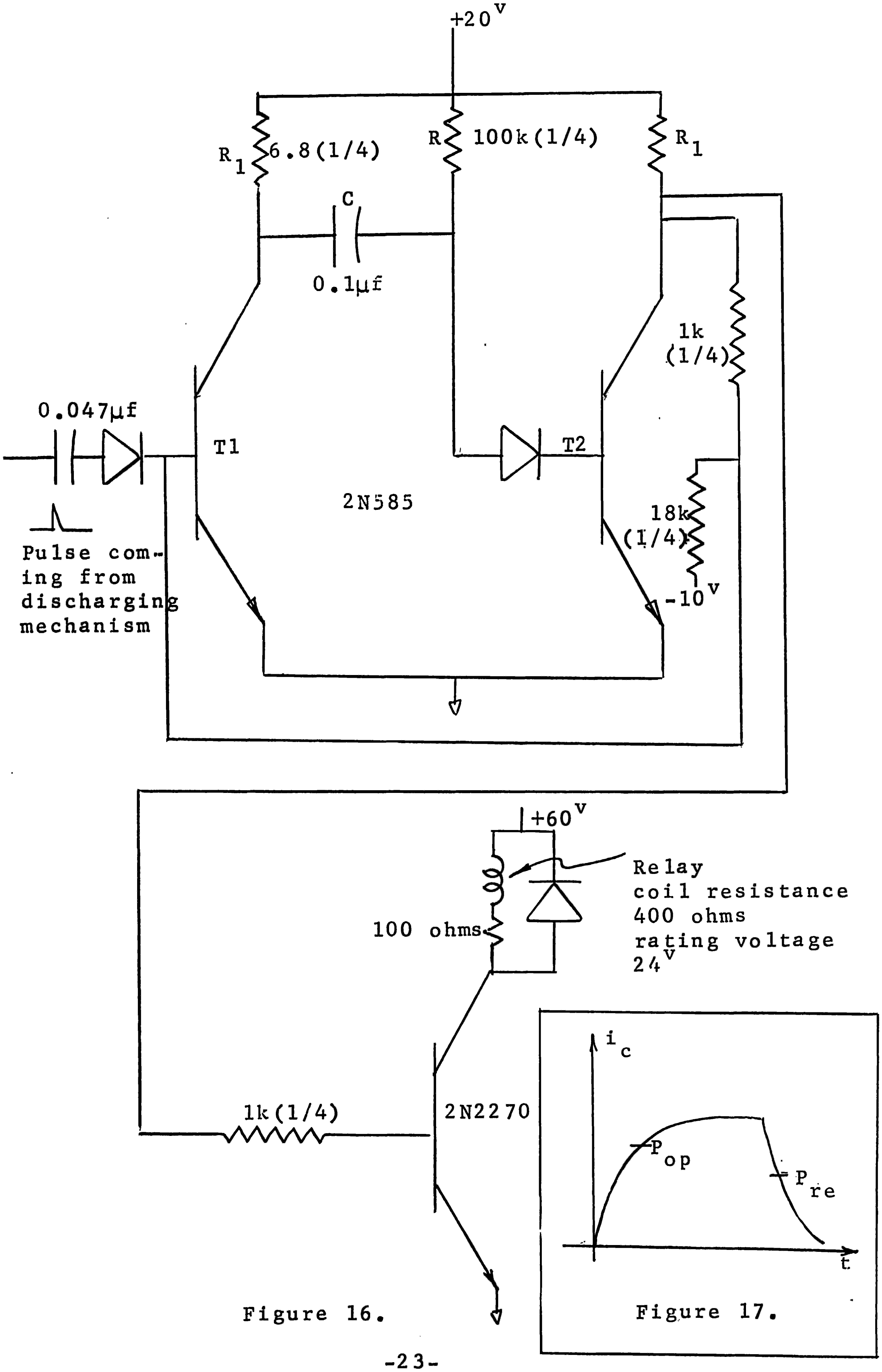


Figure 16.

Figure 17.

the rating of 24^V dc with a coil resistance 400 ohms. The general characteristics of such a relay is shown in Figure 17. When the relay is energized, it will operate if the current exceeds the operation point, P_{op}, and the relay will release if the current is less than the release point, P_{re}. The release point is lower than the operation point. In order to minimize the delay in response, the slopes of the coil current curves are required to be as steep as possible, and it is well known that the slope depends on both the time constant and the final value of current. For a given relay, the time constant is fixed, therefore changing the final value of current is the only way to minimize the delay in response. Experimentally, increasing the operating voltage to around 40^V reduces the response delay to a satisfactory value. Since the power supply available in the vicinity of 40^V is 60^V, a 100 ohms resistor in series with the relay is necessary. The corresponding output pulse width of the univibrator is about seven miliseconds,

$$RC \ln 2 = (100k)(0.1\mu f)(0.7) = 7ms$$

which is less than the one percent requirement, 10ms.

7. High Input Impedance Cathode-follower Voltmeter

In order to measure the residual voltage across C, a voltmeter is needed which should meet the following requirements:

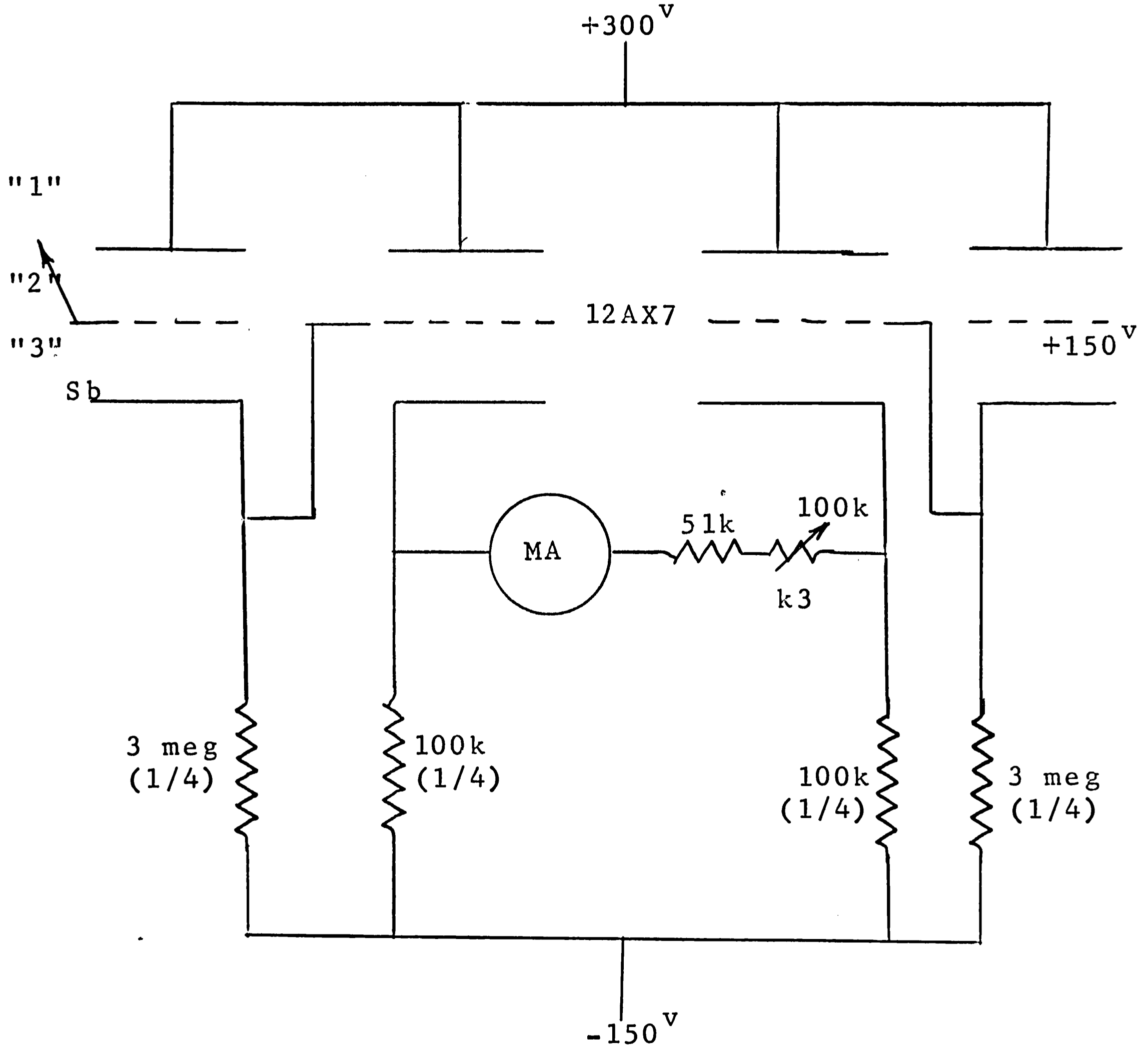
1) The input impedance must be very high in order not to load the capacitor so as to result in a changing reading on the meter.

2) It should be able to handle large input voltage swings, hence vacuum tubes are used. In addition, the grid current has to be very small as compared with the charging current, 10μA.

The circuit diagram shown in Figure 18 shows that the input stage is in fact a cathode-follower. The input impedance, therefore, is quite high thus meeting the first requirement.

In Figure 19., there are two major kinds of grid currents, i.e., the negative and positive grid currents. When the grid is negative with respect to the cathode, a current, which is the result of positive ions that are attracted to the grid, flows from the grid terminal. This is defined as the negative grid current in the conventional sense. The ionization of the residual gas in the tube depends on both the plate voltage and plate current. Hence using a reasonable plate voltage and decreasing the plate current by returning a very large cathode resistance to the negative power supply in our case can make this negative grid current quite low.

Because of the initial velocities of the thermo-electrons, many of them have sufficient energy to arrive at the grid even if it is at a considerable negative voltage with respect to the cathode and thus form the positive grid current. Since these two kinds of grid currents tend to cancel each other, the net grid current must be less than the larger one of the two component currents. As a matter of fact, it was found by the method illustrated in the following paragraph that this net grid current was negligible as compared with the plate charging current in the present case.



"1": connected to +150^V; for zero MA reading calibration

"2": connected to +60^V; for full scale MA reading calibration reference

"3": connected to the right plate of current switching stage through a 10 meg resistor (for decoupling)

Figure 18.

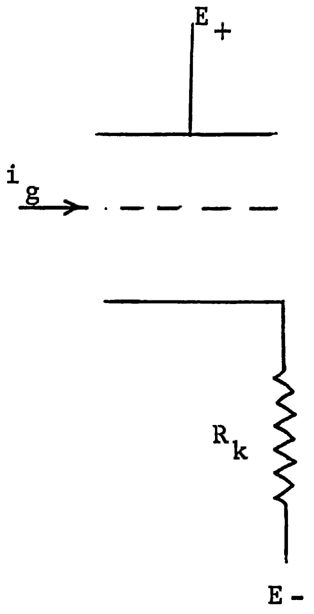


Figure 19.

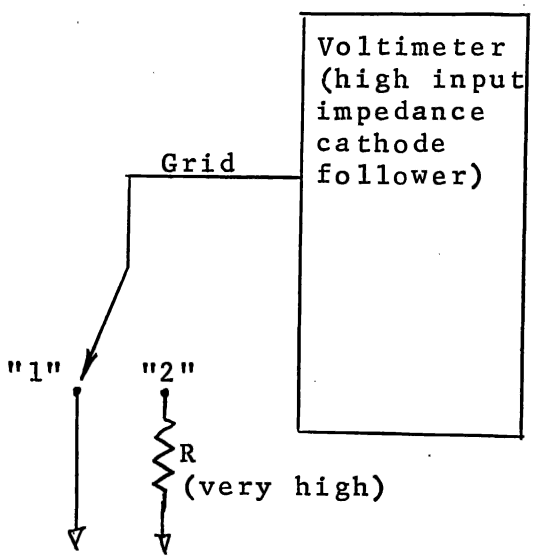


Figure 20.

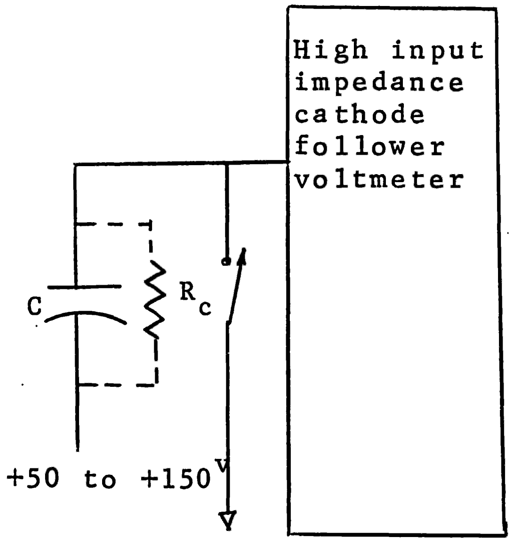


Figure 21.

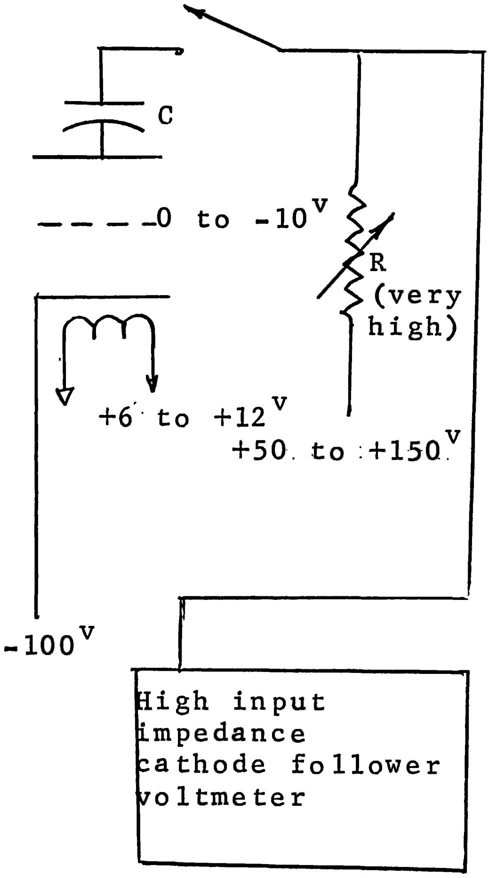


Figure 22.

The method employed to measure the grid leakage current is illustrated in Figure 20. First, the input grid was grounded and the right-hand side voltage was adjusted to get a zero reading on the milliameter MA. Then the input grid was switched to position "2". The grid leakage current flowing through 10meg resistor R produced a voltage drop which was read by the milliameter. The grid leakage current thus read fell between 10^{-9} and 10^{-10} amp. As far as the 10μA charging current is concerned, this grid leakage is negligible. In other words, the voltmeter built here is quite satisfactory.

In order to verify that the leakage current of the capacitor was sufficiently small as not to change the voltage across the capacitor over a period of several minutes. The arrangement shown in Figure 21 was used. The switch was opened after the milliameter was set to zero, and it was found that the meter reading did not change appreciably over a peroid of several minutes

So far, it has been shown that the capacitor and the voltmeter leakage currents are not troublesome, hence if there is any leakage when the tube is nominally cut off it must be the tube leakage current which was discussed in 3. This current was measured using the configuration shown in Figure 22. The process is almost the same as before; the leakage current flowing through R producing a voltage drop which can be read by the miliameter.

8. Calibration Circuits

a) Up to the present time, it has been implicitly assumed that when one section of the twin-triode 12AX7 is turned off the other will be immediately turned on in the current switching function, but this is not true. Referring to Figure 23 with the trimmer, C_t, temporarily disconnected, let us see what would happen when a series of negative pulses is applied to the grid. The grid and the cathode voltage waveforms are shown in Figure 24. Examining these waveforms reveals that the cathode voltage can not follow the leading edge of the grid waveform satisfactorily because of the stray capacity, C_{ks}, to ground, hence the counting rate of the whole device will be slowed down.

In Figure 24., point "a" is determined by the input grid voltage and the ratio of C_{ks} and the total equivalent capacitance (including the trimmer C_t) between the grid and the cathode; point "b", the conduction point where the right section of the 12AX7 begins to conduct current, is determined by the general tube characteristics under the constraints of right hand fixed bias and the constant plate current $10\mu A$. In order to improve the situation, it is desired to move point "a" downward so that the right section of the tube can conduct whenever the input grid voltage is -10^v. The change of point "a" can be obtained by adjusting the trimmer. It is worthwhile to note that when the next negative pulse comes in, point "b" is lowered because of the decrease of the plate voltage of the right section which, in turn,

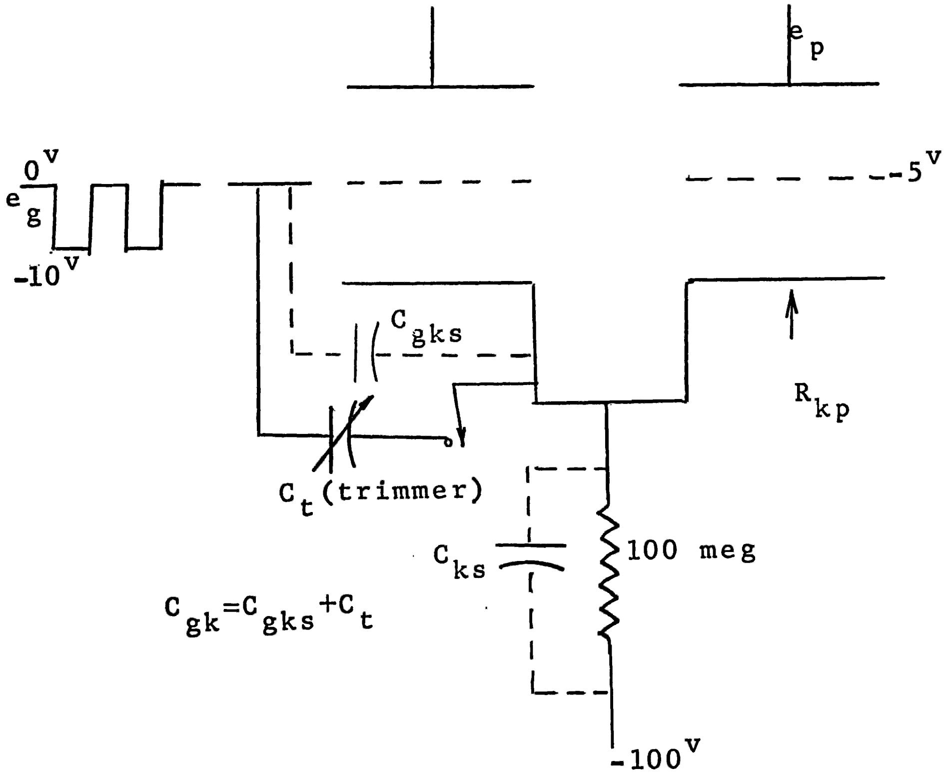


Figure 23.

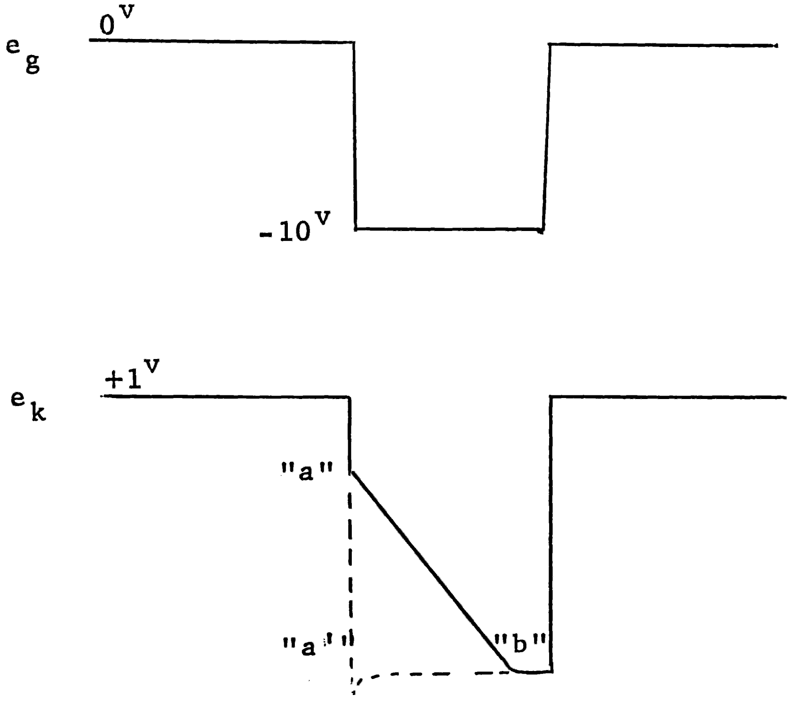


Figure 24.

results from the charge accumulated across the charging capacitor when the previous pulse was present at the left grid. As a result, points "a" and "b" can not always coincide with each other during a series of negative pulses. Therefore, a compromise of the setting of C_t must be made by try-and-error method so that the countint rate of the whole device can be the one desired.

b) In order to be able to periodically calibrate the whole device, a free-running multivibrator was designed to provide a series of equally spaced START and STOP pulses for the input flip-flops. The free-running multivibrator which runs at 50kc is shown in Figure 25. Between "a" and "b" in the figure, there is a differentiator but the negative excursions are eliminated by the diodes, the positive pulses at "b" are sent to single-stage amplifier and inverter. Furthermore, "A" and "D" are connected to the input diodes of the input flip-flops, "B" and "C" to the corresponding collectors. This forms a pulse steering network which causes the input flip-flop to be complemented for each pulse coming from the single-stage amplifier.

When these calibration circuits are used to calibrate the whole device, the counting rate is not expected to be exactly 100 counts/ 200 secs. This is because of the delay of the input flip-flop transistor in its transition from saturation to cut-off. When 500pf crossover capacitors were inserted to speed up the transition the delay was about half a microsecond. When the cross-over capacitors were removed, the delay was about two microseconds or more. Therefore, cross-over capacitors are needed and half a microsecond delay is tolerable as far as this project is concerned. The calibration counting rate is thus around 97 counts/200 secs (since the ON time is slightly less than half of the total time) when the 500pf capacitors are inserted.

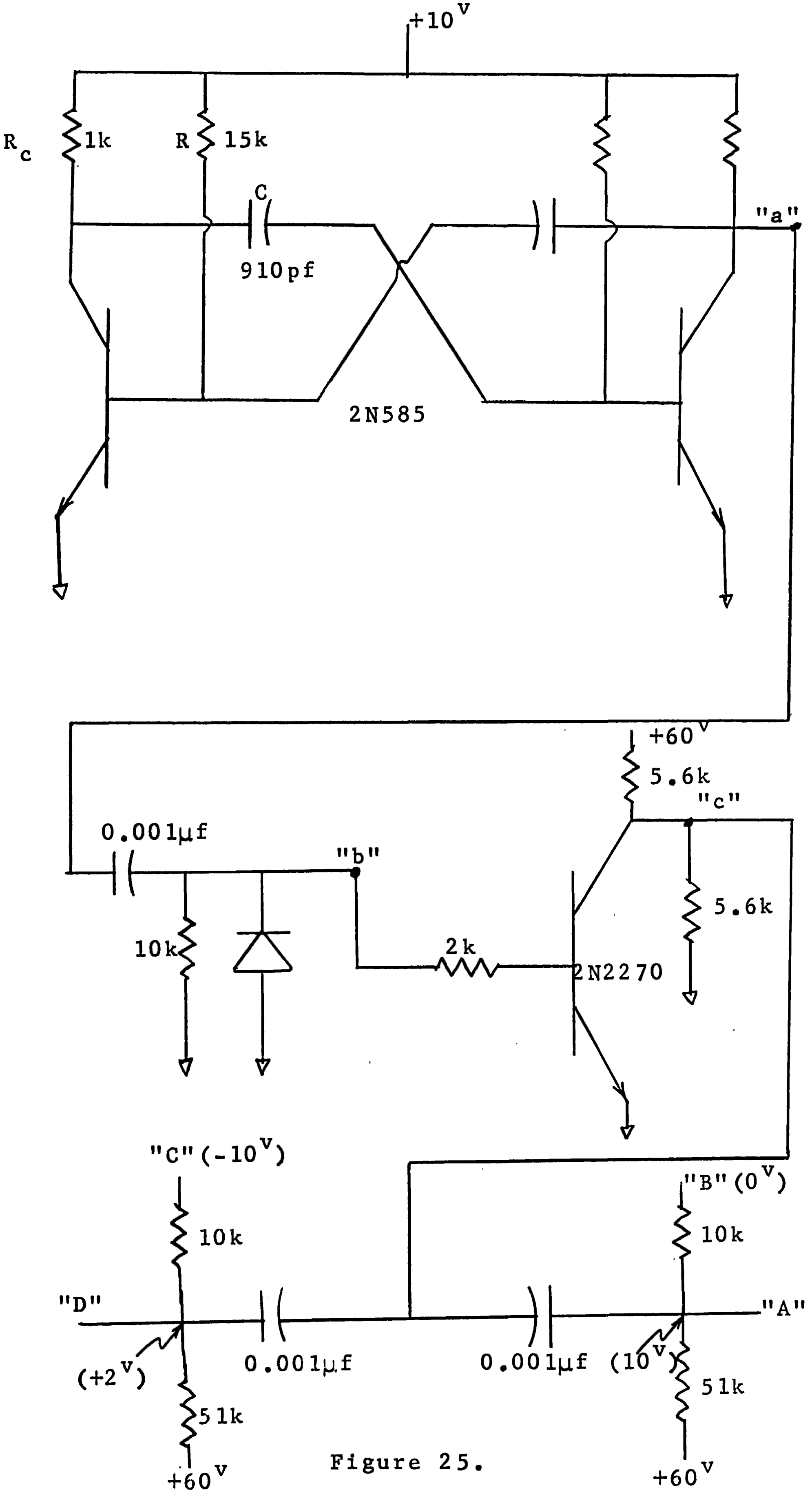

+10V
R_c
1k
R
15k
C
910pf
"a"
2N585
+60V
5.6k
"c"
0.001μf
"b"
5.6k
10k
2k
2N2270
"C" (-10V)
"B" (0V)
10k
10k
"D"
"A"
(+2V)
0.001μf
0.001μf
(10V)
51k
51k
+60V
+60V

Figure 25.

(IV) Calibration and Operation Procedure

Five channels have been built based on the circuitry described before. Channels 1 through 4 have input flip-flops, but channel 5 has both an input flip-flop and a univibrator with a switch to select the desired operation. Since only one voltmeter has been built, a channel-selection switch is necessary when the reading of each channel is needed.

The calibration and operation procedure is described in steps as follows for each channel:

(a) Set the switch in current switching stage, S_a, at position "1". Adjust the neon bulb firing control knob K1 to the point where the neon bulb fires.

(b) Set S_a at "2", adjust (slightly) the charging current control knob K2 to obtain one count per second as measured by a stop watch.

(c) Set the switch in the voltmeter section, S_b, at position "1". Adjust mechanically the zero reading of the milliameter. Then set S_b at "2", adjust K3 to make the meter reading approximately full scale.

(d) Set S_b at "3", readjust K1 and K2 to make the meter indication swing through the full scale, at the same time maintaining the counting rate one per second.

(e) Connect the free-running multivibrator for calibration to the input flip-flop and set S_a at "3". Adjust C_t to obtain 97 counts/200 secs.

(f) Repeat step (a) through (e) for each of the five channels.

(g) For the calibration of the input univibrator of channel 5, adjust R, the 50k potentiometer, to make the output be exactly 10us wide with the aid of an oscillscope.

(h) Finally when the calibration is completed, disconnect the free-running multivibrator. Then connect START and STOP signals from the appropriate circuits whose operation times are to be measured to the input terminals shown on the front panel of the monitor.

(V) The Application to the Investigation of the Rice Computer

Up to the present time, only the investigations of memory fetches and FO orders of the Rice Computer have been made. The data obtained so far are shown in the following tables. Table 1 and Table 2 show how the data were obtained step by step for FO orders and memory fetches respectively. Table 3 and Table 4 show all significant data obtained for these two kinds of operations under different programs.

1	When	2/5/64	
2	Who	Mary Shaw	
3	Total operation time	50	Sec.
4	FO	13.7	Sec.
5	CC+1	3.3	Sec.
6	Memory Fetch	8.6	Sec.
7	Time of any I-O	18.0	Sec.
8	Number of FO orders X 10 μs	6.7	Sec.
9	Number of FO orders	0.67×10^6	
10	Average of FO order time	20.4	μs
11	Actual operation time (#3-#7)	32	Sec.
12	FO/actual operation time %	42	%
13	CC+1/actual operation time %	10.2	%
14	Memory fetch/actual operation time %	27	%

Table 1.

1	When	1/5/64	
2	Who	Pat Groves	
3	Total operation time	100	Sec.
4	FO	33.1	Sec.
5	CC+1	9.1	Sec.
6	Memory Fetch	19.5	Sec.
7	Time of any I-O	12.6	Sec.
8	Number of memory fetches X 10 μs	16.7	Sec.
9	Number of fetches	1.67×10^{6}	
10	Average of fetch time	11.6	μs
11	Actual operation time (#3-#7)	87.4	Sec.
12	FO/actual operation time %	40.5	%
13	CC+1/actual operation time %	10.4	%
14	Memory fetch/actual operation time %	22.4	%

Table 2.

Who	Average of FO order time (MS)	FO/actual operation time (%)	CC+1/actual operation time (%)	Memory fetch/actual operation time (%)
Mary Shaw	20.4	42	10.2	27
Mary Shaw	18	45	11.5	29
Mary Shaw	19.6	41	3.7	26
Mary Shaw	18.3	43	12.7	30
Mary Shaw	18.5	35.8	8.4	20.5

Table.3.

Who	Average of fetch time (MS)	FO/actual operation time (%)	CC+1/actual operation time (%)	Memory fetch/actual operation time (%)
Pat Groves	11.6	40.5	10.4	22.4
Pat Groves	12.1	39	10.3	22.2
Pat Groves	11.8	34	9.7	21.8
Pat Groves	11.9	35.4	9.2	22.2
F. Baskett	11.1	26	7.4	17.2
F. Baskett	11.8	23.5	7.9	19.4
F. Baskett	11.6	23	7.6	18.9
F. Baskett	11.3	27.9	7.9	18.5
F. Baskett	11.3	27.9	7.8	18.6
Mary Shaw	10.4	39	11.1	23.5
Mary Shaw	10.4	39	11	23
Mary Shaw	10.4	40	12.8	23.6

Table 4.

(VI) References

1. Strauss, Leonard, "Wave Generation and Shaping", McGraw-Hill Book Co., 1960
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6. Related Transistor and Tube Manuals