RICE UNIVERSITY

MAGNETIC TAPE CODER AND DECODER

BY

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The need for the magnetic tape coder and decoder system and the requirements set forth for its operation are discussed. The coder output which is to be recorded serially on one channel of a frequency modulated tape recorder is in the form of four digit, binary-coded-decimal numbers in which the binary bit "0" is represented by a voltage level of +1 volt and the binary bit "1" is represented by +2 volts. The code word numbers are generated sequentially from the number 0 to the number 9999. When a code word number is to be sought at a later time in the decoding operation, the output of the tape recorder is connected to the input of the decoder and the tape is then searched. When the decoder senses the code word which is present on the dials of a Digiswitch, a relay is closed in order to perform other desired operations such as the copying of the data at any particular point of the original coded tape onto other tapes. A discussion of the system logic design is presented, followed by a discussion and analysis of the individual circuits, their waveforms, their interconnections, and their interactions with one another.
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INTRODUCTION

The need for the magnetic tape coder and decoder arose in the field of bio-medical research as an instrumentation tool to aid in the recording and analysis of such physiological data as the electroencephalogram, the electrocardiogram, galvanic skin response, and respiration, among others. The physiological data is to be studied to determine the effects of such phenomena as sleep or the lack of it, emotional states, drugs, and the presentation of photic, audio, or tactual stimuli on the experimental subject.

Because of the large amounts of magnetic tape used in large scale physiological studies, some method of marking code words on the tape is needed in order that any given position on the tape may be located rapidly upon playback of the tape at a later time. It may be desired that code words be generated at a constant rate in order to mark the passage of time. In this manner the tape may be coded at such rates as one word per millisecond, per second, or per ten seconds, as examples. Such timing of the code word generation may also be controlled so that each code word immediately precedes the presentation of a stimulus. This is important since the analysis of physiological data immediately preceding and following the presentation of an external stimulus is especially desired. The code words may thus be used as time or event markers.

It is desired that the coding be performed serially on a single recording channel so that all the remaining channels are available for recording physiological data.

In the experimental runs the data that is gathered is usually recorded on a paper strip pen recorder either directly or at a later
time by transferring the tape recording to the pen recorder. Trained observers may then examine the data for significant parameters and information. For this reason, the coding of the tape must be in such a format that the observer may visually recognize each code word in order to locate precisely the information on the recording. The coding scheme must also be suited to electronic detection as well.

Since the waveshapes of much of the physiological data are composed mainly of low-frequency components, a frequency modulated (FM) tape recorder must be used to record the data. A binary code using two different voltage levels to represent the "1" and "0" states would be ideally suited to FM recording and could easily be read by an observer on a paper strip recording.

The code that was chosen is in the form of binary-coded-decimal numbers in which a word consists of a four digit decimal number with spaces between each binary bit and larger spaces between each decimal digit so that the individual numerals of each word may be read and distinguished from one another with ease. A voltage level of +2 volts was chosen to represent the binary numeral "1" whereas the "0" was represented by +1 volt. See figure 1 for the waveshape of a typical code word. The code word numbers are written on the tape sequentially from 1 to 10,000.

In applications involving paper strip recording, the rate at which the code words are written on the paper must be slow enough to allow sufficient spacing between the binary bits so that the individual numerals may be seen by the observer. For high speed applications the rate at which the coding may be written on the tape is limited by the
Figure 1. Wavefront of the binary-coded-decimal code word number 1965.
upper frequency response of the tape recorder at the desired tape speed. In this case the detection of the code words upon playback of the tape may be performed by the decoding circuitry.

The code word number to be sought is set on the dials of a Digiswitch. When the designated word appears, a relay is closed by the decoding circuitry in order to perform any other desired operation. One such operation is the copying of valuable information contained on a particular portion of an original tape onto other tapes. The code word corresponding to the beginning of the desired portion of the tape is set on the Digiswitch. The appearance of that word causes the relay to trip and initiates the copying process.

Although sophisticated commercial models of magnetic tape coders and decoders exist in which the month, day, hour, and even fractions of a second are coded onto the tape in complicated formats involving pulse widths and pulse positions, the cost of such units runs into many thousands of dollars. The unit described above, however, is a special purpose model in which one of the primary design goals was economy consistent with reliable operation. The total retail price of the electronic components used in the prototype was less than $250.

This unit is versatile in that the code words can be made to represent time markers as well as event markers. Provisions are made for adjusting the rate at which the code words are written on the tape and the spacing between the binary bits so that the coder may be used for low speed paper strip recording or for higher speed applications. The coding format is such that the code words may be distinguished both visually and electronically.
SYSTEM DESIGN CONSIDERATIONS

The following basic requirements were to be met in order to insure operation of the magnetic tape coder. First, there must be some way of generating the code word numbers sequentially from 1 to 10,000 in binary-coded-decimal form. The obvious solution to this problem was a binary counter truncated to permit operation as a binary-coded-decimal or decade counter. A clock was necessary to provide the pulses to be counted and to determine the rate at which the different numbers were to be generated. Secondly, the number contained in the binary counter must be transferred serially from the counter to the tape. One possible solution to this problem would be the gating of the contents of the counter into a shift register which would shift the bits of the code word serially onto the tape. Instead of using a separate shift register, it is much more economical to use a single register which can be gated for operation as either a counter or shift register. Such a combination counter and shift register was used with the register connected as a ring shifter in the coding process so that after being shifted to the tape, the code word would be aligned in its original position in the register to await the addition of a "1" to produce the next code word. A clock was used to generate the pulses to shift the register. Thirdly, some means of controlling the beginning and end of the shifting process and controlling the spacing between numerals of the code word number was necessary. A scaler counter which counted the pulses of the clock used to shift the register was used with the appropriate gates connected to the outputs of the scaler.

The magnetic tape decoder had the following basic requirements.
First there was to be some means of sensing whether each incoming binary bit received by the decoder was a "1" or "0". This requirement was met by means of a pair of Schmitt triggers biased to differentiate between the two different voltage levels. Secondly, there must be some way of storing the information represented by the bits until the complete code word has been received. The shift register, which was common to the coding and decoding circuitry, performed the storing function. Thirdly, after a complete word had been stored in the register, some means was necessary of determining if the code word number was the one being sought. This task was accomplished by means of a Digiswitch connected to the register so as to compare the number stored in the register with the number selected on the Digiswitch dials. The Digiswitch would give the proper output if the two numbers were identical.

The basic design considerations of the coder and decoder have been summarized above. A description of the functional logic chosen to fulfill and integrate the above design requirements will proceed next, followed by a detailed description and analysis of the individual circuits used, the waveforms produced by these circuits, and the connections and interaction between circuits.
EXPLANATION OF CODING AND DECODING FUNCTIONAL LOGIC

The operation of the coding system is shown on the coding logic diagram of figure 2. Turning the six-pole double-throw (6PDT) code and decode mode switch to the code position activates the coding circuitry. This setting applies power to the coding circuitry, connects the register as a ring shifter, and allows the master reset switch to reset flip-flops 1 through 16 and set flip-flops 17 through 21. The first sixteen flip-flops contain the code word. The "1" states of the last five flip-flops serve as a signal to the decoding circuitry upon playback of the tape to compare the word in the register to the word selected on the Digiswitch.

Next, one selects the desired type of input circuit by turning the input selector switch to the external clock, internal clock, or feedback input position. The rate at which the sequential code word numbers are generated is determined by the frequency of the pulses entering the input switch. In the feedback position, the end of one word initiates the beginning of the next.

A word consists of four binary-coded-decimal numerals composed of 16 bits plus five additional bits as explained above. A blank space is required between each numeral and between a word and the last five bits. These blank spaces isolate each numeral to aid in visual recognition of the number. The 21 bits plus the 4 spaces make 25 counts required from the bit-pulse-generating clock in order to form one complete word.

Assume that a word has just been generated. That word will be contained in the first 16 places of the register since the register is operating as a ring shifter. The scaler will contain a count of 25
since 25 pulses from the bit-pulse-generating clock were required to form one word. Gate 1 senses a count of 25 and is inhibiting the bit-pulse-generating clock.

The pulse ordering the next word to be generated appears at the input and turns on gate 10, the "begin word" gate, which triggers the two following univibrators. Univibrator number 2 with the longer time constant, T₂, turns on gate 13, the "enable count" gate, which gates the register for operation as a binary-coded-decimal counter. There must be a sufficient delay after the activation of the "enable count" gate before the "count command" pulse is received by the counter in order to allow for the rise time and stabilization of the voltages involved in the gating operation. This delay is furnished by univibrator number 1 with the shorter time constant, T₁. When this latter univibrator returns to its stable state after a delay time, T₁, the resulting positive going wave is applied to the "count command" input of the register, thereby adding "1" to the number already in the register. This same positive going wave sets the last five flip-flops of the register. The setting of the last five flip-flops at this time is a precautionary step. If any electrical noise had entered the system and had flipped any of these five "1" states to "0", the last five states would be set and corrected at this time. The coding circuitry would be unable, however, to correct any mistakes in the first sixteen flip-flops caused by noise. Fortunately, such mistakes caused by electrical noise are very rare. Univibrator number 2 then returns to its stable state after time T₂, disabling the register as a counter and resetting the scaler. With the scaler now reset, gate 1 no longer sees a count of 25 and no longer inhibits the bit-pulse-generating clock. The initial square wave output from the clock propagates through gates
2 and 5 to gate 7, which then ceases to inhibit gates 8 and 9. The output of gate 8 changes from 0 volts to +1 volt, whereas the output of gate 9 either remains at 0 volts or becomes +2 volts, depending upon whether register flip-flop 16, containing the most significant bit of the most significant numeral of the code word, contains a "0" or a "1", respectively. A flip-flop contains a "1" or is said to be in the "1" state if the right hand transistor is cut off and its collector is at a negative voltage. Otherwise the flip-flop contains a "0".

Gate 12 is an emitter follower whose output is equal to the largest of the voltages appearing at the outputs of gates 8 and 9.

The trailing edge of the initial square wave clock pulse propagates through gate 11, the "shift command" gate which causes the register to shift one place to the left. The same trailing edge of the clock pulse causes gate 2, the "scaler count" gate to send a positive pulse to the "count" input of the scaler which then contains a count of one. At the same time, gate 7 is caused to inhibit gate 8 and 9 and the output of gate 12 returns to zero volts, thereby completing the generation of the first code bit at the output of the coder.

The above process is repeated as each successive bit is shifted around the ring shifter into flip-flop 16. After the first four bits, representing the most significant decimal numeral, are coded, the scaler contains a count of 4 and activates gate 3 which prevents a print-out at the output and a shifting of the register. Thus, a blank space appears on the tape between the first coded numeral and the second numeral. Gate 3 is similarly activated after counts of 9, 14, and 19 to yield spaces after each decimal numeral. At the count of 25 gate 1 turns off the clock and the number which was contained in the regis-
ter has been written on the tape.

When the master reset switch is switched to the reset position the first 16 flip-flops of the register and the entire scaler are reset whereas the last five flip-flops of the register are set to a "1" state. The bit-pulse-generating clock is turned off by gate 1 since -15 volts from terminal "a" of the reset switch appears at the input of gate 1. The instant the reset switch is switched in the other direction, the number zero followed by five "1"'s appears at the output of the coder. The coding of all the numbers from 1 to 10,000 sequentially follows the coding of the first number, zero.

The decoding logic diagram is shown in figure 3. In order to make the unit operate as a decoder, the code-decode mode switch is turned to the "decode" position. In this position, power is applied to the coding circuitry. The register, gate 11, and univibrator number 3 are used in both modes of operation and are connected directly to the power supplies. Gate 13 of the coding circuitry is also directly connected to the power supplies. In the decoding mode, gate 13 disables the counting circuitry of the register and allows the register only to shift. The mode switch also connects the register as a straight through shifter so that each time the register shifts one place to the left, a "0" appears in flip-flop 1. In this manner, a "0" always appears in the first flip-flop whenever a code-word bit appears at the decoder input. If the bit happens to be a "1", then the circuitry described below sets a "1" into the flip-flop, and the mode switch allows the master reset switch to reset flip-flop 17 so that upon resetting the register, only the last four flip-flops contain a "1". All the other flip-flops contain a "0".
DECODER LOGIC DIAGRAM

0 VOLTS = RESET FLIP-FLOPS 1-17
SET FLIP-FLOPS 18-21

SHIFT REGISTER

FLIP-FLOPS 17-21 ARE IN "0" STATE

OUTPUTS, FLIP-FLOPS 1-16
WORD SENSING GATE

32PDT FORWARD AND REVERSE SWITCH

DIGISWITCH

RESET

MASTER RESET SWITCH

RUN

-15V

INHIBIT CLAMP TO GND.

"1" LEVEL DETECTOR

"0" LEVEL DETECTOR

UNIVIBRATOR NUMBER 3

SHIFT COMMAND GATE

SHIFT COMMAND

SET FLIP-FLOP 1

RESET FLIP-FLOPS 1 + 17

NO WORD BIT AT INPUT

UNIVIBRATOR NUMBER 4

-15 V

RELAY

WORD IS IN REGISTER

WORD IS CORRECT

NO WORD BIT AT INPUT

AND GATE

DECOR DRIVER

APPLY POWER TO DECODING CIRCUITRY

CONNECT REGISTER AS STRAIGHT-THROUGH SHIFTER

ALLOW MASTER RESET TO RESET FLIP-FLOP 17

CODE-DECODE MODE SWITCH

FIGURE 3
The code pulses are fed from the tape recorder directly into the input amplifier which amplifies the pulses and inverts their polarity. The amplified pulses are then applied to the input of the level detectors. The "1" voltage appears at the output of the amplifier. The "0" level detector is a Schmitt trigger which triggers if either the larger "1" voltage or the smaller "0" voltage appears at the amplifier output. When a level of less than 1 volt appears at the amplifier input, both level detectors return to their initial state.

Suppose the first bit of a word appears at the input of the decoder. The "0" level detector triggers and the leading edge of its output triggers univibrator number 3, driving gate 11, the "shift command" gate, which shifts the register one place to the left. A "0" now appears in flip-flop 1. If the first word bit is a "1", then the "1" level detector triggers. The trailing edge of the "1" bit causes the "1" level detector to return to its initial "0" state, generating a positive pulse which sets a "1" into the first flip-flop. Flip-flop 1 now contains the first bit of the code word. The above process is carried out for each bit of the code word.

The decoder circuit is designed to close a relay to initiate desired operations in the playback and analysis of the recorded data. The relay will close if register flip-flops 1 through 16 contain the designated word, flip-flops 17 through 21 contain a "1", and no word bit is present at the input of the decoder. The correct word must be preceded by five "1"'s. It will be remembered that in the coder, each generated word is followed by five "1"'s. But then, of course, each word on the tape will be preceded by five "1"'s except the first word which is the number zero. The first word, the number zero, is considered to be a dummy word and will not be detected by the decoder.
As the word bits shift through the register to the left, one place at a time, gate 14, the "word sensing" gate, senses the outputs of flip-flops 17 through 21. When five "1"s appear in these places, gate 14 senses that a word is present in the register and activates one of the three inputs of gate 15, the decoder "and" gate. The Digiswitch senses the outputs of the first 16 flip-flops. When the word it senses matches the word preselected on its dials, the second input of the decoder "and" gate is activated. The word in the register, however, is not complete until the trailing edge of the last bit of the code word, which is the least significant bit of the code word, appears at the input of the decoder. The "0" level detector returns to its "0" state, flip-flop 1 either remains in a "0" state or is set to a "1" state, and the third input of the decoder gate senses that no word bit is present at the input. When the three input conditions of gate 15 are met, gate 15 activates gate 16, the relay driver which clamps one end of the relay coil to the ground, thereby causing the relay to close.

If the word in the register were not the correct word, then the relay would remain open, but gate 17, the "wrong word" gate, would be activated, triggering univibrator number 4. After a short delay, determined by the univibrator time constant, $T_u$, the trailing edge of the univibrator resets flip-flops 1 and 17. With these two flip-flops reset to "0", it is impossible, in the decoding of the next word, to have five "1"s in flip-flops 17 through 21 except when a bona fide word is present in the first 16 flip-flops. This step prevents gate 14, the "word sensing" gate, from giving a false output. Gate 14 will then sense only the five "1"s normally between each word.
It will be seen that the "wrong word" gate is activated every time a word has entered the register. Suppose the word which has just entered the register is correct. The "wrong word" gate is activated and triggers univibrator number 4. At the same time the relay driver clamps one end of the relay coil to ground. The R C circuitry of the univibrator is also clamped to ground, so as to prevent the univibrator from returning to its stable state. Flip-flops 1 and 16 thus retain their state. The output of the input amplifier is also clamped to ground, thereby preventing the shifting of the register and preserving the state of flip-flop 1. Thus, when the correct word appears in the register, this word is retained in the register and the relay closes. The relay remains closed until the master reset switch is flipped to the reset position. The reason the master reset switch is made to reset flip-flop 17 in the decoding mode is so that the word sensing gate will not initially see five "1"s and falsely cause the relay to close if the Digiswitch dials are set to the number zero. In this manner if the Digiswitch dials are set at zero, the relay will close on the arrival of word number 10,000 since the first zero is a dummy word.

If one desires to decode the tape when the tape recorder is in reverse direction, the "forward and reverse" switch is switched to the "reverse" position, thereby inverting the order in which the flip-flop outputs of the first 16 flip-flops are connected to the Digiswitch.

The reasons for the choice of five "1" bits between each code word to activate the "word sensing" gate is explained more fully below. The decoder circuitry will not compare the word in the register with the word selected on the Digiswitch until the inter-word code mark appears in the "word sensing" gate. The inter-word code mark must then
be some series combination of bits which is not a code word numeral. One such possibility would be a series of four "1"'s or the binary number 1111. Such a code mark, however, has certain limitations. These limitations arise when there are flaws on the tape or when the decoding process is begun in the middle of the tape rather than at the beginning.

It may be seen that even though not a possible code word itself, the binary number 1111 may be formed in a code word bit series. The maximum number of "1"'s which can occur consecutively in a binary-coded-decimal code is four. These four "1"'s occur when the numeral seven is followed by the numerals eight or nine as in the number 78, which in binary-coded-decimal form is 0111 1000.

The type of trouble which may occur is described in the following example. Suppose the code word number 7800 preceded by the inter-word mark of four "1" bits is about to enter the decoder from the tape. The sequence of bits would be 1111 0111 1000 0000 0000. These twenty bits, beginning with the bits of the inter-word mark, 1111, would be placed sequentially into the first flip-flop of the register and would be shifted sequentially along the register from right to left. Suppose that because of noise or a flaw on the tape, any one of the "1"'s of the inter-word mark failed to be recorded as a "1". Then when the above twenty bits had entered the counter, the "word sensing" gate would not sense the first four bits as being an inter-word mark, since one of them would fail to be a "1". The decoder circuitry would not compare the word in the register with the word set on the Digiswitch, nor would the "wrong word" gate cause univibrator number 4 to reset the register flip-flops. At this time in the circuit of this example, the first and also
every fourth register flip-flop would have had to be reset to avoid the possibility of the "word sensing" gate sensing four "1"'s, produced by the juxtaposition of the two code word numerals when the next word entered the register. The inter-word mark with the mistake and the number 7800 would then continue being shifted into the register. When the four "1"'s produced by the juxtaposition of the numerals seven and eight reached the "word sensing" gate, the gate would falsely sense these four "1"'s as being an inter-word mark and would cause the contents of the register to be compared with the number on the Digiswitch thereby causing the possibility of a false decoding since the bits of the actual code word, 7800, have been displaced five places to the left in the register. If the register word comparison had not caused a false operation of the relay at this time, the register flip-flops would then be reset. Since the code word bits had been displaced five places to the left, the next four bits to enter the register after the resetting of the register would be "1"'s, again caused by the juxtaposition of the numerals seven and eight. This error would continue recurring until the numeral seven was no longer followed by an eight or a nine. The last such number would be 7999. Thus a single flaw on the tape could invalidate as many as 200 code words following the flaw.

This same type of error could occur again between the code word numbers 0780 and 0799, 1780 and 1799, etc., yielding 200 extra possibilities for error. Similarly, between the numbers 0078 and 0079, 0178 and 0179, etc., an additional 199 possibilities for error may occur.

If one of the "1" bits of the inter-word mark had been obliterated not by a flaw on the tape but rather by beginning the decoding process in the middle of an inter-word mark, then the same possibilities
for error discussed above could occur if the next code word to enter the register contained a seven followed by an eight.

Another series of possible decoding errors could occur if only the first bit of the inter-word mark were obliterated preceding any code word from 8000 to 9999. As an example, consider the binary-coded-decimal form of the number 8000 preceded and followed by the inter-word mark of four "1"'s, l11l 1000 0000 0000 0000 1111. Suppose that for some reason the first bit of the first inter-word mark were obliterated so as to yield 0111 1000 0000 0000 0000 1111. When the code word enters the register, the "word sensing" gate fails to sense that a word is present in the register. Only after the register has shifted once more and the code word is displaced one position to the left does the "word sensing" gate yield an output. If the bits in the register at this time match the number selected on the Digiswitch, an error in the decoding will occur. If the words do not match, then register flip-flop 1 and every fourth flip-flop would be reset. Since the code word in the register at this time had been displaced one place to the left, the first "1" bit of the next inter-word mark would then be in register flip-flop 1 and hence would be reset to zero, causing the very same error to occur in the decoding of the code word number 8001 that occurred in the word 8000. The same error would occur in all the following numbers up to the number 9999 unless another "1" bit in the inter-word mark were obliterated in the meantime.

There is one other type of error to be considered. Suppose that a flaw on the tape caused an extra "1" to appear in the inter-word mark preceding any code word. As an example consider the binary-coded-decimal form of the code word number 7802 preceded by the inter-word mark containing an extra "1". The bit series would be l11l1 0111 1000
0000 0010 1111. The bits would enter the register by being shifted sequentially one place to the left. When the first four "1"'s reached the "word sensing" gate, a possible decoding error could occur. If the bit series in the register were not those of the word being sought, then register flip-flop 1 and every fourth flip-flop would be reset. The next series of four "1"'s would be the one preceding the code word number 7703 and the coding process would be correct from then on. Therefore, only the word immediately following the inter-word mark with the extra "1" bit could be decoded with a possible error.

Some of the possibilities of error discussed above can be eliminated by the choice of five "1"'s for the inter-word mark. In this case if any of the "1" bits of the inter-word mark were obliterated preceding a code word number less than 8000 in which a seven is followed by an eight or nine, there would be no possibility for a decoding error since as was seen earlier the maximum number of "1"'s that can occur in series in a binary-coded-decimal coded is four. The "word sensing" gate then would not see five "1"'s and only the word which was preceded by the obliterated inter-word mark will be ignored in the decoding process.

The inter-word mark of five "1"'s is still subject to the same type of error in the code words 8000 through 9999 as was described above in the case of an inter-word mark of four "1"'s if the first bit of the inter-word mark is obliterated.

The inter-word mark of five "1"'s was the one chosen for the decoding unit. Although the possibilities for error discussed above are definite limitations of the system, the chances of such errors be-
ing produced are exceedingly small. The chance of a flaw occurring on the tape is very small. The chance that the flaw will occur at the very spot on the tape at which the first bit of an inter-word mark occurs is much smaller and the operation of the decoder can be considered to be very reliable.

Another favorable consideration of an inter-word mark of five "I"s is that the capacity of the system may be increased by departing from the decimal system and truncating the register counter to count in binary coded form to as high as the base twelve if so desired. Of course the appropriate Digiswitch would have to be used.

In a number system to the base thirteen or higher, there is a possibility of obtaining more than five "I"s in the juxtaposition of two numerals. By adding another flip-flop to the register and using an inter-word mark of six "I"s, one may use a numbering system to as high as the base fourteen.

In the case of an inter-word mark of five "I"s, only the first and seventeenth register flip-flops have to be reset to "0" after the comparison of a word in the register with the word on the Digiswitch in order to insure that the only series of five "I"s entering the register during the loading of the next code word into the register would be that of the inter-word mark.
DESCRIPTION AND ANALYSIS OF THE MAGNETIC TAPE CODER AND DECODER CIRCUITRY

The following preliminary specifications apply to all the circuitry in this section. All resistors have a tolerance of five percent. Although most of the resistors used in the prototype have a power rating of one-half watt, the power dissipation was low enough to permit the use of one-quarter watt resistors in all circuits except gate 13, which will be explained later.

With the exception of the unijunction transistor type 2N2160 used in the internal unijunction clock and the high voltage type 2N398A used in gate 13, all PNP transistors are switching type 2N707 and all NPN transistors are switching type 2N587. All diodes are type 1N281. In the switching circuits, the minimum beta required to insure saturation of the transistors in each circuit was calculated. The betas of the transistors actually used were at least twenty percent greater than the minimum value needed to insure saturation. In this manner the effect of such factors as resistance tolerance and small variations in the power supply voltage are minimized.

Plus and minus fifteen volt supplies delivered power to all the circuits except the "enable count" gate which used a minus thirty-five volt supply in the collector circuit of the high voltage transistor type 2N398A. The fifteen volt power supplies were connected to the circuits used exclusively in the coding process through terminals d and e of the code-decode mode switch. Power to circuits used exclusively in the decoding process was supplied through terminals q and r of the code-decode mode switch. The circuits used in both the coding and decoding process were connected directly to the power supplies. In
the circuit diagrams which follow, the letter in parenthesis by the
circuit power terminals indicates to which point of the code-decode
mode switch the terminals are connected. If no letter in parenthe-
sis appears by the power terminal of a circuit, then this circuit
is connected directly to the power supply.

The heart of the coder and decoder is the register which
can be gated to operate as either a counter or a shift register. Figure
4 shows a circuit diagram of one of the first sixteen flip-flops
of the register. The interconnections between the flip-flop ter-
\[\text{minal points are shown in figures 5, 6, and 7. If the right hand}
\]
transistor, Q2, is on, the transistor is saturated, the collector
is at zero volts, and the flip-flop is said to be in the "0" state.
Actually there is a collector to emitter voltage drop of about 0.1
volt. This value is typical for the transistor type 2N404 which was
used. As far as the circuitry to which the flip-flops are connected
is concerned, the collector voltage is negligible and may be consid-
ered to be at 0 volts. If Q2 is cut off, the collector is at either
-7 volts or -8.2 volts, depending upon whether the input to point h
is 0 volts or -30 volts respectively, and the flip-flop is said to be
in the "1" state.

Consideration shall now be given to the transistor betas re-
quired in the flip-flop circuitry. Referring to figure 4, assume Q1
is saturated. Q2 will then be cut off. The base, b of Q1, is connec-
ted to the network composed of R1, R5, R3, R8, and R12. Assume point
h is at -30 volts. Looking into the above network, one finds a
Thevenin equivalent voltage source of -3.7 volts in series with a
Thevenin equivalent resistance of 4K. With a base to emitter voltage
Figure 1. Schematic of one of the first sixteen bistable multivibrators of the register.
drop of 0.3 volts, the Thevenin equivalent circuit will deliver .85 milliamperes into the base of Q2 to ground. A current of 2.94 milliamperes must flow through the collector resistor R2 in order to insure saturation. The minimum beta necessary to insure saturation is then the ratio of the collector current to the base current, 2.94 ma./.85 ma., which equals 3.5. Transistors with betas of 50 or above were used in the flip-flops thereby establishing a considerable margin of safety in insuring saturation to offset such factors as tolerance variations in component values and variations in the power supply voltage.

The counting operation of the register is performed by the register's first sixteen flip-flops as follows: Assume point h of figure 4 is held at 0 volts by gate 13. Further assume the flip-flop is in a "0" state so that point C2 is at 0 volts. Point m will then be at 0 volts and point n will be at -5.3 volts due to the voltage divider operation of resistors R7 and R11 and of R8 and R12. It is seen that points m and n are either at or approximately at the collector voltage levels. Hence points m and n act as steering points for the inputs at points d and e. If a voltage level change of +7 volts, equal in magnitude to the voltage level change of a collector of the flip-flop in figure 4 when the flip-flop changes states, is applied to point d, a positive pulse of approximately the same magnitude appears at point b, with a time constant of 8.3 microseconds determined by capacitor C3 and resistors R7 and R11. This positive pulse turns off Q1 and the regenerative action of the flip-flop turns on Q2. Now if the voltage level change of +7 volts had been applied to point e, the state of the flip-flop would remain the same since Q2 was already cut off. If points d and e are joined and a voltage level
change of +7 volts is applied to the junction point, the flip-flop will change states every time the positive voltage change appears at the junction point.

Figure 5 shows the interconnections of the first four flip-flops, which allow binary-coded-decimal counting operation. These first four flip-flops contain, in binary-coded form, a decimal numeral which corresponds to the least significant decimal numeral of the code word number. The next four flip-flops contain the next numeral, etc. Points h of the flip-flops of figure 5 and one end of the 20K resistor are joined at point x and are held at 0 volts by gate 13 for counting operation.

The -15 volt power supply must be connected to points j and k of the flip-flops for operation. Points j are connected directly to the power supply. Points k are connected to the power supply through a pole of the master reset switch. The flip-flops of the counter are reset by flipping the master reset switch to the "reset" position. In this position, the minus power supply is disconnected from points k of the counter flip-flops. Points k are then left floating. Under these conditions, no current is able to flow through R3 of figure 4. Point b1 is held positive and Q1 is cut off by R1 and the positive power supply. The current from point j through R2 and R6 into b2, turns on Q2. Thus the flip-flops are in a "0" state. When the master reset switch is switched to the "run" position, the flip-flops are in a "0" state and are operative.

Every time a positive going wave appears at the "count command" input of figure 5, FF1 (flip-flop number 1) changes state. At every second input pulse, a positive going wave appears at c2 of FF1
Figure 5. Interconnections of register counting circuitry of first four bistable multivibrators operating as decade counter.
and complements the next stage. This same positive going wave is propagated from \(c_2\) of FF1 to d of FF4. A positive pulse at d would reset FF4. This fourth flip-flop, however, is already in a reset or "0" state. Hence FF4 does not change state until a positive going wave appears at point e. Only after eight pulses have appeared at the "count command" input does a positive going wave appear at point e of FF4. Hence FF4 remains in a "0" state through a count of seven. At the count of eight FF4 switches states and contains a "1". The negative pulse propagating at this time through capacitor \(C_0\) of figure 5 has no effect on the other circuitry since only positive going waves can cause the flip-flops to change state. At the count of nine FF1 changes to a "1" state. The next input pulse must cause all four flip-flops to contain a "0" to insure binary-coded-decimal operation. Just prior to the count of ten, FF1 and FF4 contain a "1" whereas FF2 and FF3 contain a "0". At the count of ten, FF1 changes to a "0" state. The positive going wave which then appears at \(c_2\) of FF1 is propagated to point d of FF4 and resets FF4 to "0". This same positive going wave, however, simultaneously appears at points d and e of FF2 and tends to cause this flip-flop to change to a "1" state. This latter change must be prevented since the four flip-flops must be in a "0" state at this time.

The change is prevented as follows: It was seen that at the count of ten, FF4 changes to a "0" state and, hence, a positive going wave appears at \(c_2\) of FF4. This positive going wave is propagated through capacitor \(C_0\) and through diode \(D_0\) to \(b_1\) of FF2 which is the flip-flop that is tending to change to a "1" state. The positive pulse at \(b_1\) of FF2 tends to cause FF2 to change to a "0" state. Since the
time constant determined by $R_0$ and $C_0$ in figure 5 is roughly twice as large as the time constant determined by $C_3$, $R_7$, and $R_{11}$ of figure 4, more energy is delivered to point $b_1$ than to $b_2$ of FF2 and hence FF2 is forced into a "0" state. The four flip-flops are now reset. The above resetting process which took place upon the count of ten occurred at a speed determined by the fall times of the transistors in the flip-flops. The fall time of these transistors is on the order of 0.3 microsecond. At this short duration any voltage change occurring at $c_2$ of FF2 will not deliver enough energy to cause FF3 to change state. Hence at the count of ten, the four flip-flops of figure 5 are reset and remain reset until the next pulse is received at the input of the counter.

The manner in which the flip-flops containing the coded decimal numerals are connected together is shown in figure 6. Each block represents a group of four binary-coded-decimal flip-flop counters shown in figure 5. At the count of ten, the voltage at point $c_2$ of FF4 in figure 5 swings positively. In figure 6 this latter positive going wave is shown to propagate to the input of the next decade counter. In a like manner, FF12 in figure 6 changes state after every 100 input pulses to FF1 and FF16 changes state after every 1000 input pulses to FF1.

The manner in which the counting operation of the register is inhibited may be seen in figure 4. Point h is brought to -30 volts by gate 13 during the period of time in which the register is to be used as a shifter instead of a counter. Assume the flip-flop contains a "0". Point $c_2$ is then at 0 volts and point $c_1$ is at -8.2 volts, the Thevenin equivalent voltage determined by the voltages at points h and j and resistors $R_{11}$, $R_7$, $R_2$, and $R_6$. The voltage divider formed by
Figure 6. Interconnections of register decade counters.
R7 and R11 holds point m at -12.1 volts. Point n is held at -5.3 volts by the voltage divider of R8 and R12. When a flip-flop in the register changes from a "1" state to a "0" state, a positive going 8.2 volt wave is propagated to the counting input of the next stage. In figure 5, the positive going wave would appear at the junction of points d and e in the case of FF1, FF2, or FF3. In FF4, the wave would appear at point e only. In propagating through the input coupling capacitors C3 and C4 of figure 4, the loading caused by the steering resistors drops the input pulse from 8.2 volts to less than 7 volts at points m and n. Of course in FF4 in figure 5, the loading at input e alone is not as great and the pulse at point n is dropped to slightly over 7 volts. The value of the peak absolute voltage appearing at points m and n is obtained by adding the peak value of the pulse propagating through capacitors C3 and C4 to the dc voltage level already present at points m and n. It was seen above that the dc voltage level at point m is -12.1 volts. The incoming positive pulse which is on the order of 7 volts does not raise point m to a positive level and the state of Q1 is not affected by this pulse. The dc level of -5.3 volts at point n, when added to the incoming positive pulse, yields about +1.7 volts at point n. When propagating through diode D2 an additional voltage drop of half a volt across the diode reduces the magnitude of the positive pulse reaching the base of Q2 to the order of +1 volt. This latter pulse is too small and of too short duration to supply enough energy to cause Q2 to change states. In figure 5 it was shown that in the counting operation, when FF4 changes to a "0" state, a positive pulse propagated through capacitor C6 and diode D0 to point b1 of FF2. However, when point x is held at -30 volts, the junction
of $R_Q$ and $C_Q$ is also at -30 volts and the pulse propagating through $C_Q$ cannot raise the junction of $R_Q$ and $C_Q$ to a positive level. Hence all counting operation is inhibited when point x is held at -30 volts by gate 13.

The shifting operation of the register flip-flops is not affected by the voltage level at point h of figure 4. Every time a "shift command" pulse is delivered to point a, the steering resistors $R_9$ and $R_{10}$ which are connected to the collectors of the previous stage determine what state the flip-flop will assume.

Figure 7 shows the interconnections of the register shifting circuitry. Assume FF1 contains a "1" and FF2 contains a "0". Point $C_2$ of FF1 holds point f of FF2 at -18 volts. Point g of FF2 is at 0 volts. When a shift pulse is applied to point a of the register FF2, the steering resistors $R_9$ and $R_{10}$ of FF2 cause the base of $Q_1$ to go positive by about 6.5 volts and causes $Q_1$ to turn off. FF2 is then in a "1" state. The contents of FF1 are shifted one place to the left to FF2. In a like manner the contents of each flip-flop in figure 7 are shifted one place to the left.

As mentioned previously, the last five flip-flops, FF17 through FF21, are in a "1" state and are used to allow the decoder to sense the end of a code word. These last flip-flops do not function as counters but operate only as part of the shift register. A circuit diagram of one of the last five flip-flops is shown in figure 8.

Points f and g of FF1 and FF21 in figure 7 are connected by the code-decode mode switch so as to allow the register to operate as a ring shifter in the coding operation as explained earlier. The connections of FF1 and FF21 to the code-decode mode switch for decoding
Figure 8. Schematic of one of the last five bistable multivibrators of the register.
Figure 7. Interconnections of register shifting circuitry.
will be explained in a later section.

The maximum frequency at which the shift register would reliably shift was found to be 25,000 shifts per second. Although the register counter operated much faster than this, the maximum frequency at which the coder could operate was limited to the generation of 25,000 bits per second or 1000 code words per second.

The scaler counter will be discussed next. The circuit diagram of a typical scaler flip-flop is shown in figure 9. The flip-flops are interconnected as shown in figure 10. The scaler is connected as a straight binary counter with a feedback path from point c1 of FF3 to points b2 of FF1 and FF2. Every time FF3 changes to a "1" state, FF1 and FF2 are also changed to "1" states by the positive pulse propagating through capacitor C1. A "1" state corresponds to a collector voltage of -7.2 volts.

The scaler truth table showing the states of each flip-flop after every input count pulse is shown in figure 11. The output voltages of the scaler flip-flops are used in gating other circuitry functions which are explained later. The scaler is reset in a manner identical to that of the register.

Figure 12 shows the circuitry of the master reset switch. The switch is a double pole, double throw (2PDT) microswitch. When the switch is in the "reset" position, pole number 1, p1, connects +7 volts to the unijunction clock and causes the clock to be in an inoperative state. Pole number 2 connects -15V to input number 1 of gate 1 and causes gate 1 to inhibit the bit-pulse-generating clock. Point c of the reset switch is then floating. The counting flip-flops of the scaler and register are reset, whereas the last five register flip-
Figure 9. Schematic of one of scalar bistable multivibrators.
Figure 10. Interconnections of scaler bistable multivibrators.
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<th>5</th>
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Figure 11. Scaler truth table.
Figure 12. Master reset switch
flops are set as explained earlier. When the reset switch is switched to the "run" position, the negative power supply is connected to points j and k of the register and scaler flip-flops and these flip-flops become operative. A voltage of +15 volts is applied to the unijunction clock and causes it to begin operation.

The code-decode mode switch is shown in figure 13. In the "code" position, poles p₁ and p₂ connect the plus and minus power supplies to the power inputs of all circuitry involved in the coding process. Poles p₃ and p₄ connect the steering resistors of the first register flip-flop, FF₁, to the collectors of the last register flip-flop, FF₂₁. Under these conditions, when a "shift command" pulse is received by the register, the first flip-flop assumes the state of the last flip-flop. The contents of the register thus shift around in a ring and the information stored in the register is preserved. The preservation of the contents of the register is essential to the sequential generation of code word numbers. Poles p₅ and p₆ allow the master reset switch to set FF₁₇ of the register so that the last five flip-flops are in a "1" state. In this manner, each code word is followed by five "1"'s which serve as word markers. The connections formed by the code-decode mode switch in the decade position will be explained later in the description of the decoding circuitry.

The first step in initiating the coding process is the selection of the "code" position on the code-decode mode switch. Next, the type of input circuitry desired to initiate the generation of each code word is selected on the input selector switch shown in figure 14. The pole of this switch is connected to the input of gate 10, the "begin word" gate which initiates the starting of each code word. One of
Figure 13. Code-decode mode switch.
Figure 14. Input selector switch and gate 10, the "begin word" gate.

Figure 15. Internal unijunction clock
three input circuits may be selected. The first position of the input selector switch connects to the external clock input which may be driven by such devices as manually controlled switches or cam driven switches for precise timing operation. The input signal must be a voltage level change or pulse which goes positive in order to cut off the transistor in the "begin word" gate which is biased to saturation by the negative supply through resistor $R_2$.

The second position of the input selector switch connects to the output of the internal unijunction clock shown in figure 15. When set for the fastest pulse rate of 1000 pulses per second, the unijunction clock yields output pulses with a peak value of +5 volts. Gate 10 is designed to switch for input levels of +2 volts or greater. With +2 volts applied to the input of gate 10, the transistor base input network of $R_1$ and $R_2$ at point b has a Thevenin equivalent voltage source of +1.5 volts in series with a Thevenin equivalent resistance of 9.09K. The +1.5 volts is sufficient to cut off the transistor and put the collector, point c, at -15 volts. When the input of gate 10 is held at 0 volts, the Thevenin equivalent voltage at point b of the transistor input network is -1.36 volts. The voltage drop from the base of the transistor to ground is about -0.3 volts. The current which flows into the base of the transistor is then 0.117 milliamps. A collector current of 2.94 milliamps needed to saturate the transistor requires a minimum beta of 25.2.

The above calculations illustrate the manner in which the minimum transistor beta is determined for all the transistor gates in the coding and decoding circuitry.

The output pulse frequency of the unijunction clock shown in
figure 15 is determined by the R C circuitry connected to the emitter of the unijunction transistor. Three ranges of frequency may be obtained by selecting the position of the word rate range switch. The frequency may be continuously varied over each range by varying the value of rheostat R\textsubscript{1} by means of the word rate dial. With the switch in position 1, the output pulse frequency may be varied from 1 pulse per second to 11 pulses per second. In position 2 the frequency may be varied from 10 pulses per second to 110 pulses per second. In position 3 the frequency may be varied from 100 pulses per second to 1100 pulses per second. The essential operation of the unijunction transistor is as follows: When the voltage at the emitter, \( e \), with respect to the base 1, \( b_1 \), of the transistor is less than a certain voltage, defined as \( E_{\text{max}} \), the resistance from \( e \) to \( b_1 \) is very large and the transistor is cut off. When the voltage from \( e \) to \( b_1 \) reaches the value of \( E_{\text{max}} \), the resistance from \( e \) to \( b_1 \) becomes very small and the transistor conducts. When the voltage from \( e \) to \( b_1 \) then drops below another value, \( E_{\text{min}} \), the transistor then cuts off and will not conduct until \( E_{\text{max}} \) is again reached. In the circuit of figure 15, when the transistor is cut off, the voltage level at \( b_1 \) is approximately +1 volt due to leakage current through \( R_4, R_3 \), and the transistor. With the particular transistor used, conduction occurred when the emitter voltage reached +10 volts. The transistor cut off when the emitter voltage fell below approximately +7 volts. This latter voltage varied slightly with the firing rate of the transistor.

When the master reset switch is in the "reset" position, a voltage of +7 volts, corresponding to \( E_{\text{min}} \), formed by the voltage divider \( R_1 \) and \( R_2 \) in figure 12 is applied to point a of the unijunction clock which is thereby cut off. When the reset switch is flipped to
the "run" position, point a of the clock is connected to the +15 volt supply and the voltage across the capacitor in the R C charging network of the unijunction transistor begins to charge toward +15 volts with a charging rate determined by the value of the capacitance chosen by means of the word rate range switch and the resistance of \( R_1 \) plus \( R_2 \). When the voltage at the emitter reaches +10 volts, the transistor fires and the emitter capacitor discharges rapidly through the emitter to base 1 junction through \( R_4 \) producing a voltage pulse across \( R_4 \) at point \( b_1 \). When the emitter voltage falls to +7 volts, the transistor cuts off, the output voltage pulse ceases, and the emitter capacitor begins to charge again. The smaller the capacitance is chosen on the range switch and the smaller the resistance is adjusted by \( R_1 \), the faster the charging rate becomes and the greater the output pulse frequency becomes.

The third choice of input circuits at the input selector switch is the "feedback" gate of figure 16. In this circuit, the input diodes are connected to points \( C_2 \) of scaler flip-flops FF4 and FF6. Point a of the "feedback" gate is held at the more positive of the two input voltages. If either or both FF4 and FF6 are in a "0" state, point a will be held at 0 volts. Only if both FF4 and FF6 are in a "1" state does point a assume a negative voltage corresponding to a "1" state of the scaler flip-flop, which is -7.2 volts. Referring to the scaler truth table of figure 11, it is seen that FF4 and FF6 are both in a "1" state only at the count of 25 at which time a code word has just finished being generated. At this time the base of the transistor in the "feedback" gate is held at a negative voltage by the voltage divider \( R_2 \) and \( R_3 \) thereby cutting off the transistor.
Figure 16. Gate 4, the "feedback" gate.

Figure 17. Univibrator number 1
A voltage of +15 volts is thereby connected to point 3 of the input selector switch through the collector resistance $R_4$ of the "feedback" gate. When the scaler is reset at the beginning of the generation of the next code word which was initiated by the positive going wave of the "feedback" gate, FF4 and FF6 are in a "0" state and point a of the "feedback" gate is held at 0 volts.

With point a held at 0 volts, the Thevenin equivalent circuit of the input network delivers 0.092 milliamps into the base of the "feedback" gate transistor. A minimum beta of 32 is required to saturate the transistor.

It was seen that when a positive voltage was applied to the input selector switch by one of the input circuits, the "begin word" gate yielded a negative going wave. Univibrators number 1 and 2 are made to trigger from this latter negative going wave. The schematics for univibrators number 1 and 2 are shown in figures 17 and 18.

Figures 19a and 19b illustrate the output voltage waveforms of the two univibrators. At time $t_1$, the "begin word" gate triggers both univibrators and the voltages at points $c_2$ go negative. The waveform at point $c_1$ of univibrator number 2 is the inverse of that at point $c_2$. The voltage at point $c_1$ of the univibrator number 2 goes to zero at time $t_1$ and activates gate 13, the "enable count" gate which gates the register for counting operation. At time $t_2$, after a 20 microsecond delay in order to allow the gating voltages at the "enable count" input to stabilize, univibrator number 1 returns to its stable state. The resulting positive going wave at point $c_2$ causes the register to count, thereby adding "1" to the number already contained in the register. The same positive wave sets a "1" into the
Figure 18. Univibrator number 2
**Figure 19 a.** Output voltage waveforms at point $c_2$ of univibrator number 1

**Figure 19 b.** Output voltage waveforms at point $c_2$ of univibrator number 2 with $C_1 = 0.001 \text{ mf}$
last five flip-flops of the register as an insurance against noise. At time \( t_3 \) after an 80 microsecond delay univibrator number 2 returns to its stable state. The resulting positive going wave at point \( c_2 \) resets the scaler. The counting function of the register is disabled at this time.

The delay of 80 microseconds in univibrator number 2 was obtained by setting the delay selector switch in figure 18 to position 3 which connects a 0.001 microfarad capacitor into the timing circuitry. Position 2 of the delay selector switch yields a delay of 800 microseconds whereas position 1 yields a delay of 8000 microseconds. The delay selector switch was incorporated into the circuitry of univibrator number 2 to be used with the "feedback" gate input circuitry. The delay between the end of generation of one code word and the beginning of generation of the next code word can be selected to suit the selected code word bit pulse width. In this manner if the tape is being coded at a slow rate, a long delay can be selected for univibrator number 2 to allow sufficient time for the trailing edge of the last bit of a code word to reach 0 volts before the initiation of the next code word.

Capacitor \( C_3 \) of figure 17 and capacitor \( C_b \) of figure 18 are speed-up capacitors to sharpen the output waveforms of the univibrators. A minimum beta of 24 is required to insure saturation of the transistors in the univibrators.

Gate 13, the "enable count" gate, is shown in figure 20. Point a of the input is connected to point \( c_1 \) of univibrator number 2 and goes from a negative voltage to 0 volts when the univibrator is triggered. The voltage of the base of transistor \( Q_1 \) of the "enable
to pt. $c_1$ of univibrator number 2

Figure 20. Gate 13, the "enable count" gate.

Figure 21. Gate 1, the "inhibit clock" gate.
count" gate then goes positive, cutting off \( Q_1 \) and thereby turning on and saturating \( Q_2 \). Transistor \( Q_2 \) is high voltage type 2N398A which is able to withstand the -35 volts in the collector circuit. When \( Q_2 \) turns on, point \( c_2 \), which is connected to the register "enable count" input, goes to 0 volts and allows the register to count the positive pulse entering the "count command" gate. When univibrator number 2 returns to its stable state, point \( a \) of the "enable count" gate goes negative, turning on \( Q_1 \) and cutting off \( Q_2 \). The output of \( Q_2 \) is connected to point \( h \) of register flip-flops 1 through 16. The resulting resistive load loads down point \( c_2 \) of the "enable count" gate to -30 volts which is the proper voltage for disabling the counting function of the register. A collector current of 116 milliamps must flow through \( R_5 \) in order to saturate transistor \( Q_2 \). Transistor \( Q_1 \) acts as a buffer amplifier to supply the necessary base current without loading down univibrator number 2. When \( Q_1 \) is turned off, the resistive network of \( R_3 \), \( R_4 \), and \( R_5 \) causes 9.7 milliamps to flow into the base to emitter junction of \( Q_2 \) thereby requiring \( Q_2 \) to have a minimum beta of 12 in order to saturate. Transistor \( Q_1 \) must have a minimum beta of 34 to insure saturation. Capacitor \( C_1 \) is a speed-up capacitor used to sharpen the leading and trailing edges of the output waveform.

The power rating of the 300 ohm resistor \( R_6 \) of the "enable count" gate will be discussed next. When \( Q_2 \) is saturated, the 116 milliamps of collector current dissipates slightly over 4 watts of power in \( R_6 \). The 4 watts of power are dissipated only for the length of time that univibrator number 2 is in its unstable state. This length of time is determined by the delay selector switch setting. Ordinarily the shortest delay setting is used with the internal unijunc-
tion clock or external clock input circuitry. With the shortest delay of 80 microseconds, the worst case average power dissipation will occur at the fastest coding rate of 1000 words per second or one millisecond per word. During each millisecond period, 4 watts will be dissipated in $R_g$ for 80 microseconds. During the remainder of the period the 5 volt drop across $R_g$ dissipates only 0.083 watts. The average power dissipation for the one millisecond period is then 0.4 watts.

If by chance the delay selector switch of univibrator number 2 is turned to position 1 for the longest delay of 8 milliseconds and the code word bits are being generated at the fastest rate of 25,000 pulses per second, then $R_g$ will dissipate 4 watts most of the time. Therefore, in order to be safe, $R_g$ should have a power rating of at least 4 watts.

The resetting of the scaler by univibrator number 2 starts the generation of the next code word by causing gate 1 to stop inhibiting the bit-pulse-generating clock.

Gate 1, the "inhibit clock" gate is shown in figure 21. The bit-pulse-generating clock will run only if the transistor of the "inhibit clock" gate is saturated. If this latter transistor is cut off, the bit-pulse-generating clock is inhibited. The "inhibit clock" gate transistor will cut off if the inputs to the gate are such that the base of the transistor goes negative. The base will go negative if the master reset switch is in the "reset" position in which case $R_4$ is returned to -15 volts. The base will also go negative if the scaler contains a count of 25. If either points 1 or 2 are at 0 volts, point a of gate 1 will be held at zero volts. Only if both points 1 and 2 are negative will point a go negative. Referring to the scaler
truth table, points $c_2$ of scaler $FF4$ and $FF6$ will both go negative only at the count of 25. A minimum beta of 19 is required to saturate the transistor of gate 1.

The bit-pulse-generating clock is shown in figure 22. The clock is an astable multivibrator whose frequency is controlled by varying the $R\ C$ time constant in the base circuit. The value of the capacitance may be varied by the bit rate range switch which is a double pole, triple throw switch. With this switch in position 1, the clock frequency may be varied from 25 cycles per second to 300 cycles per second by means of the bit rate dial which varies the resistance of a 250 K dual potentiometer. In position 2, the frequency may be varied from 250 to 3000 cycles per second. In position 3, the frequency may be varied from 2500 to 30,000 cycles per second. It should be remembered, however, that the shift register operates only up to 25,000 cycles per second.

The emitter of $Q_1$ of the bit-pulse-generating clock is connected to the collector of gate 1. When the transistor of gate 1 is cut off, no current can flow in $Q_1$ of the clock. Clock transistor $Q_2$ saturates and point $c_2$ is held at 0 volts. As soon as gate 1 allows the clock to run by clamping point $c_1$ of the clock to ground, the clock immediately changes its state and point $c_2$ goes positive. The resulting waveform is shown in figures 23, 25 and 27, together with waveforms of associated circuitry.

Figures 23 and 24 contain an expanded portion of the waveforms corresponding to the first numeral and interdigit gap of a generated code word. At time $t_{11}$ in figures 23 and 24, the waveforms are repeated again at times $t_{21}$ and $t_{31}$ for the third and fourth numerals.
Figure 22. Bit-pulse-generating clock.
Figure 23. Output voltage waveforms of bit-pulse-generating clock, gate 2, and gate 3 during generation of first numeral of code word.
Figure 24. Output voltage of gate 5, gate 7, and gate 11 during generation of first numeral of code word.
of the code word. The waveforms for the inter-word mark are shown in figures 25 and 26. The first bit of the inter-word mark begins at time \( t_{41} \) and the code word generation is ended at time \( t_{50} \). Figures 27 and 28 show an overall view of the waveforms for an entire code word.

It is seen that after 25 cycles, the bit-pulse-generating clock is inhibited by gate 1 until the beginning of the next code word. A minimum beta of 150 is required for saturation of the clock transistors. High beta transistors were used to insure saturation and reliable operation for the wide range of resistance in the base circuitry.

The bit-pulse-generating clock directly drives gate 2, the "scaler count" gate shown in figure 29. The output of gate 2 is connected to the "count" input of the scaler and to input 1 of gate 5, the "print" and "shift" gate driver.

The printing of the first bit of the code word onto the tape is accomplished as follows: Notice that the output of gate 2 is connected to the input of gate 5, whose output is connected to the input of gate 7, the "print inhibit" gate. As seen by the waveforms of figures 23 and 24, when the output of the bit-pulse-generating clock goes positive at time \( t_1 \), the output of gate 2 goes negative and causes the output of gate 5 to go positive which in turn causes the output of gate 7 to go to zero. Whenever the output of gate 7, which is connected to point a of gate 8, the "0" gate, and to point 2 of gate 9, the "1" gate, goes to zero, the inhibition of gates 8 and 9 is released, gate 8 yields an output of +1 volt, and gate 9 yields an output of +2 volts or 0 volts depending upon whether register flip-flop 16 contains a "1" or a "0" respectively. Gate 12, the "emitter-follower," yields an output voltage equal to the larger voltage at either of its inputs. When the
Figure 25. Output voltage waveforms of bit-pulse-generating clock, gate 2, and gate 3 during generation of inter-word mark.
Figure 26. Output voltage of gate 5, gate 7, and gate 11 during generation of inter-word mark.
Figure 27. Overall view of waveforms for bit-pulse-generating clock, gate 2, and gate 3 for one complete word.
Figure 28. Overall view of waveforms for gate 5, gate 7, and gate 11 for one complete word.
Figure 29. Gate 2, the "scalar count" gate.

Figure 30. Gate 5, the "print" and "shift" gate driver.
output voltage of the bit-pulse-generating clock returns to zero, at
time \( t_2 \), the output of gate 2 goes from \(-14\) volts to 0 volts and the
resulting positive going wave places a count of 1 into the scaler as
shown in figure 23. The output of gate 7 goes to +14 volts and satu-
rates the transistors of gates 8 and 9 thereby inhibiting their opera-
tion. The output voltage of gate 13 goes to zero and the printing of
the first code word bit onto the tape is completed.

Notice that the output of gate 5 is also connected to input
b of univibrator number 3. At time \( t_2 \), the output voltage of gate 5
is a negative going wave which triggers univibrator number 3 which in
turn drives gate 11, the "shift" gate and causes the register to shift
one place to the left.

At time \( t_3 \) the bit-pulse-generating clock output voltage goes
positive again as shown in figure 23, thereby repeating the entire pro-
cess described above by which the code word is printed onto the tape.
The above process is repeated at every positive excursion of the bit-
pulse-generating clock until time \( t_8 \), at which time the scaler con-
tains a count of 4 and thereupon activates gate 3 as shown in figure
23. The output of gate 3 is connected to input 2 of gate 5. When the
output voltage of gate 3 goes to zero, the output voltage of gate 5 is
inhibited as shown in figure 24, thereby preventing a print out of a
code word bit at gate 13 at time \( t_9 \) and a shifting of the register at
time \( t_{10} \). At time \( t_{10} \) the scaler contains a count of 5 and gate 3
ceases inhibiting gate 5. At the next positive swing of the bit-pulse-
generating clock output at time \( t_{11} \), the waveforms shown in figures 23
and 24 from \( t_1 \) to \( t_{11} \) repeat themselves from \( t_{11} \) to \( t_{21} \), from \( t_{21} \) to \( t_{31} \),
and from \( t_{31} \) to \( t_{41} \) to form the four numerals of the code word. Gate 3
inhibits gate 5 to prevent printing and shifting from times \(t_8\) to \(t_{10}\), \(t_{18}\) to \(t_{20}\), \(t_{28}\) to \(t_{30}\), and \(t_{38}\) to \(t_{40}\). From \(t_{40}\) to the end of the code word, gate 3 no longer inhibits gate 5. It is during this time that the inter-word mark of five "1"'s is generated. The waveforms of the associated circuitry are shown in figures 25 and 26. It is seen that from time \(t_{40}\) to \(t_{50}\), each time the bit-pulse-generating clock goes positive, a "1" is printed and each time the clock goes to zero, the register is shifted and a count is added to the scaler. When the scaler receives a count of 25, gate 1 inhibits the bit-pulse-generating clock and the code word generation has been completed.

The circuitry described above will be explained more fully below. Gate 2, the "scaler count" gate, is shown in figure 29. Gate 2 inverts the polarity of the bit-pulse-generating clock so that every time the clock output goes to zero, the positive going wave at the output of gate 2 adds a count of 1 to the scaler. A minimum beta of 27 is required to saturate the transistor of gate 2.

The output of gate 2 is connected to input 1 of gate 5, the "print" and "shift" gate driver shown in figure 30. The transistor base of gate 5 is biased by \(R_1\), \(R_2\), and \(R_3\) such that as long as input 2 is held at a negative voltage by gate 3, the transistor will cut off every time the output of gate 2 goes negative and will saturate every time the output of gate 2 goes to zero. If, however, the output of gate 3 goes to zero, the transistor of gate 5 will remain in saturation regardless of the voltage at input 1 and gate 5 is thus inhibited. A minimum beta of 26 is required to saturate the transistor of gate 5.

Gate 3 is shown in figure 31. If either or both inputs 1 and 2 are held at a negative voltage, point 3 will be at a negative voltage.
Figure 31. Gate 3, "inhibit" gate.

Figure 32. Gate 7, the "print inhibit" gate.
Only when both inputs are at 0 volts will point 3 be at 0 volts and inhibit gate 5. In order for input 1, which is connected to point \( c_1 \) of scaler flip-flop 3, to be at 0 volts, flip-flop 3 must contain a "1". In order for input 2, which is connected to point \( c_2 \) of scaler flip-flop 6, to be at 0 volts, flip-flop 6 must contain a "0". Referring to the scaler truth table of figure 11, it is seen that both inputs of gate 3 will be at 0 volts at the scaler counts of 4, 9, 14, and 19 at which time gate 5 is inhibited and prevents the printing and shifting operation.

The output of gate 5 is connected to the input of gate 7, the "print inhibit" gate, shown in figure 32, which controls the printing out of the code word bits. Gate 7 inverts the phase of gate 5. A minimum beta of 18 is required to insure saturation of the transistor of gate 7.

The output of gate 7 is connected to point \( a \) of gate 8, the "0" gate, and to point 2 of gate 9, the "1" gate. Gate 9 is shown in figure 33. The base of the transistor is biased by \( R_1, R_2, \) and \( R_3 \) such that when point 2 is held at 0 volts by gate 7, the transistor is cut off if register flip-flop 16 contains a "1" or is saturated is flip-flop 16 contains a "0". If the transistor is cut off, the output, point \( c \), yields +2 volts, formed by the voltage divider \( R_4 \) and \( R_5 \). If point 2 is held at +14 volts by gate 7 then the transistor of gate 9 is saturated regardless of the voltage at point 1, which is the output voltage of register flip-flop 16. Thus when the output voltage of gate 7 goes to zero, the "1" gate yields +2 volts if there is a "1" in flip-flop 16 and yields 0 volts if there is a "0" in flip-flop 16. A minimum beta of 11 is required to insure saturation of the transistor.
Figure 33. Gate 9, the "1" gate.

to pt. \( c_2 \) of register FF16
to pt. \( c \) of gate 7

Figure 34. Gate 8, the "0" gate.

to pt. \( c \) of gate 7
Gate 8, the "0" gate, is shown in figure 34. Every time gate 7 causes point a of the "0" gate to go to 0 volts, the output of the "0" gate yields +1 volt, formed by the voltage divider $R_3$ and $R_4$. A minimum beta of 24 is required to insure saturation of the transistor.

Gate 12, the "emitter-follower output" gate is shown in figure 35. The output voltage is equal to the largest of the voltages at either input. The possible input voltages are +1 volt, +2 volts, and 0 volts. Gate 12 combines the output voltages of the "0" gate and the "1" gate to form the complete code word. The resistor $R_1$ is used as a current limiting resistance to protect the transistor in case the output is accidentally grounded. There are no strict requirements as to the beta of the transistor. A transistor with a beta of 20 or greater will work well.

The shifting of the register in the coding process occurs whenever a negative going wave from gate 5 triggers univibrator number 3 shown in figure 36. The output of gate 5 is connected to point b of the univibrator. The other input to the univibrator is used in the decoding process. Univibrator number 3 is connected directly to the power supplies since it is used in both the coding and decoding functions. The period, determined by $C_4$ and $R_6$ is 5.8 microseconds. A minimum beta of 24 is required to saturate the transistors.

Univibrator number 3 directly drives gate 11, the "shift command" gate shown in figure 37. Gate 11 is a complementary emitter-follower which must drive the shift inputs of the 21 flip-flops of the register. The complementary emitter-follower maintains a low impedance output for the positive going portion of the output waveform of univibrator number 3 as well as the negative going portion. The current limi-
Figure 35. Gate 12, the emitter follower output gate.

to pt. c of gate 9

2

D2

to pt. c of gate 8

1

D1

2N585

coder output

+15 V (d)

R1

200 ohms

R2

10 K

Figure 36. Univibrator number 3.

to pt. c2 of "0" level detector

to pt. c of gate 5

+15 V

R4

5.1 K

C3

150 pf

R5

51 K

R6

120 K

R7

5.1 K

C1

2N585

Q1

C4

70 pf

2N585

to pt. a of gate 11

R1

10 K

R2

10 K

R3

100 K

-15 V
Figure 37. Gate 11, the "shift command" gate.

to pt. c₂ of univibrator number 3

R₁ 3 K
C₁ 001 µF

2N585 c₁

Q₁ e to register "shift command" input

Q₂

R₂ 27 K

2N404

-15 V

+15 V

R₃ 200 ohms

Figure 38. Gate 6, the "end of word" gate.

to pt. c₂ of scalar FF3

to pt. c₂ of scalar FF4

to pt. c₂ of scalar FF5

1

R₁ 39 K
C₁ 500 pf

2

R₂ 39 K

3

-15 V (r)

R₄ 5.1 K

C

"end of word" output

+15 V (q)

R₃ 150 K

R₄
ting resistor $R_3$ protects the transistors in case the output of gate 11 is accidentally shorted. Capacitor $C_1$ is a speed-up capacitor used to sharpen the output waveform. A beta of 20 or greater for the transistors is sufficient. Gate 11 is connected directly to the power supplies since this gate is used in both the coding and decoding functions.

Gate 6, the "end of word" gate shown in figure 38 yields a positive going wave after the first four numerals of the code word have been generated. This positive pulse may be used to initiate the presentation of a stimulus to a subject immediately after the generation of a code word, not including the inter-word mark of five "1"s. Point a of gate 6 must go negative in order to saturate the transistor and produce a positive going wave at the output of the gate. Point a will go negative when inputs 1, 2, and 3 go negative. Referring to the scaler truth table, flip-flops 3, 4, and 5, which are connected to the inputs, contain a "1" at the count of 19 corresponding to the last bit of the code word numeral. It is seen that gate 6 as well as gate 1 and gate 4 have diode input logic in order to prevent loading of the register and scaler so as not to decrease their reliability at high speeds.

When the unit is to be used in the decoding mode, the code-decode mode switch is turned to the "decode" position. In this position, power is applied to the decoding circuitry. Register flip-flop 17 is connected so as to be reset by the master reset switch. This last step insures that gate 14 will not falsely sense a word when the register is reset. Also in the "decode" position, point g of register flip-flop is connected to -15 volts and point f of the same flip-
flop is connected to ground. In this configuration, the shift regis-
ter no longer is a ring shifter but becomes a straight-through shif-
ter with a "0" being set into the first flip-flop every time the regis-
ter shifts due to the connections of the steering resistors of the
first flip-flop as described above.

The output signal of the coded tape is fed into the input of
the input amplifier shown in figure 39. The amplifier is biased
such that with no signal in, the base and collector of the transis-
tor are very nearly at 0 volts. When the input goes positive, the
transistor output swings negative and yields a voltage amplification
of 3.5 when connected to the inputs of the level detectors. The tran-
sistor used had a beta of 50.

The "0" level detector shown in figure 40 is a Schmitt trig-
ger whose input is biased such that the circuit triggers when the
negative input voltage at point a exceeds 2 volts in magnitude. When
the voltage then drops below 1.8 volts, the circuit returns to its
original state. Point c2 is normally at approximately -1 volt. When
the "0" level detector triggers, transistor Q2 cuts off and point c2
swings to the -15 volt supply voltage.

The "1" level detector shown in figure 41 is a Schmitt trig-
ger whose input is biased such that the circuit triggers when the
negative input voltage at point a exceeds 5.2 volts in magnitude and
returns to its original state when the input voltage then drops below
5 volts. Except for the biasing resistor R2, the circuitry of the
two level detectors is identical.

The output of the "0" level detector is connected to input a
of univibrator number 3 shown in figure 36. When a code word bit ap-
Figure 39. Input amplifier.

Figure 40. The "0" level detector.
Figure 43. Output voltage waveforms of input amplifier and gate 11.
pears at the input amplifier, the "0" level detector immediately trig-
gers and delivers a negative pulse to input a of univibrator number 3. Since univibrator number 3 triggers from negative pulses, the output of the univibrator at this time causes gate 11 to shift the register one place to the left. The waveforms of the output voltage of the ampli-
plier and the output voltage of gate 11 when a word enters the de-
coder input is shown in figure 43. It is seen that after a "1" bit appears at the decoder input, a "1" is set into register flip-flop 1 when the incoming "1" bit voltage returns to 0 volts. A zero is set in flip-flop 1 whenever the register shifts. The above process is repeated for each incoming word bit. As the incoming code word shifts sequentially through the register, gate 14, the "word sensing" gate shown in figure 42, senses the output of the last five flip-flops of the register. Point 6 of gate 14 will be at a negative voltage if any of the last five flip-flops contain a "0". Only when these flip-
flops all contain a "1" does point 6 of gate 14 go to 0 volts.

The output of gate 14 is connected to point b of gate 17, the "wrong word" gate shown in figure 44. When a word is present in the register, point b of gate 17 is held at 0 volts. When the last bit of the code word input returns to 0 volts, the "0" level detector holds point a of the "wrong word" gate at -1 volts. The transistor of the "wrong word" gate is biased such that under the above conditions, the transistor cuts off.

The resulting negative going wave at the output of gate 17 then triggers univibrator number 4 shown in figure 45. If the word in the register is not the word being sought, univibrator number 4 returns to its stable state after a time delay of approximately 10
to pt. \( c \) of input amplifier

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Figure 41. The "1" level detector.

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to pt. \( c_1 \) of register FF17
to pt. \( c_1 \) of register FF18
to pt. \( c_1 \) of register FF19
to pt. \( c_1 \) of register FF20
to pt. \( c_1 \) of register FF21

to pt. \( b_2 \) of register FF1

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Figure 42. Gate 14, the "word sensing" gate.
Figure 44. Gate 17, the "wrong word" gate.

Figure 45. Univibrator number 4.
microseconds. When the univibrator returns to its stable state, the positive going wave at point \( Q_2 \) resets register flip-flops 1 and 17 as explained earlier. If the word in the register was the word being sought, then the closing of the relay would have caused point d of univibrator number 4 to be clamped to zero by the relay driver transistor. With point d at 0 volts, the base of transistor \( Q_2 \) will be held positive by the voltage divider \( R_7 \) and \( R_8 \) since \( R_8 \) is returned to +15 volts. Transistor \( Q_2 \) then will be cut off and the univibrator will be inhibited from returning to its original stable state. Thus the word in the register will not be reset.

Univibrator number 4 may be triggered falsely by gate 17 if transient voltage spikes occur at input b of gate 17. Voltage transients are likely to appear at the output of gate 14 when the register shifts. For this reason capacitor \( C_1 \) was used in the circuitry of input b of the "wrong word" gate to filter out any sharp transient voltages.

The states of the first 16 flip-flops of the register are sensed by the Digiswitch. Figure 46 shows the relationship between the dial settings and the input terminal connections for each cell of the Digiswitch. The Digiswitch, the "forward and reverse" switch, and the collectors of register flip-flops 1 through 16 are shown in figures 47 through 50. The connections were made according to the information given in figure 46 for each Digiswitch dial setting. For example, when the number zero is selected on the "units" dial, the common point c is connected internally by the Digiswitch to input terminals \( \bar{1}, \bar{2}, \bar{4}, \) and \( \bar{8} \). The "units" numeral is contained in the first four register flip-flops. Assume the "forward and reverse" switch is
<table>
<thead>
<tr>
<th>DIGISWITCH DIAL SETTING</th>
<th>INPUT TERMINALS TO WHICH POINT C OF THE DIGISWITCH IS CONNECTED</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1  2  4  8</td>
</tr>
<tr>
<td>1</td>
<td>1  2  4  8</td>
</tr>
<tr>
<td>2</td>
<td>1  2  4  8</td>
</tr>
<tr>
<td>3</td>
<td>1  2  4  8</td>
</tr>
<tr>
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<td>1  2  4  8</td>
</tr>
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<td>1  2  4  8</td>
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<tr>
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<td>1  2  4  8</td>
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<td>7</td>
<td>1  2  4  8</td>
</tr>
<tr>
<td>8</td>
<td>1  2  4  8</td>
</tr>
<tr>
<td>9</td>
<td>1  2  4  8</td>
</tr>
</tbody>
</table>

Figure 46. Relationship between Digiswitch dial settings and input terminal connections.
in the "forward" position. If the number contained in the first four flip-flops is a zero, all four flip-flops will be in a "0" state and the collectors \( c_2 \) of the flip-flop transistors \( Q_2 \) will be at 0 volts. The collectors \( c_2 \) of the first four flip-flops are joined to the Digiswitch terminals \( 1, 2, 4, \) and \( 8 \) through diodes \( D_4, D_3, D_2, \) and \( D_1 \) respectively. Terminal \( c \) will thus be at 0 volts. If any other number were present in the first four flip-flops, at least one of the flip-flops would be in a "1" state and terminal \( c \) would be at \(-8.2 \) volts corresponding to the collector voltage of a register flip-flop in a "1" state. Only if the number selected on the Digiswitch dial matches the number contained in the first four register flip-flops does terminal \( c \) have an output of 0 volts. Otherwise terminal \( c \) will be at \(-8.2 \) volts. If it is desired to play the tape in a reverse direction in the decoding process, the "forward and reverse" switch is turned to the "reverse" position and the Digiswitch terminals are thus connected to register flip-flops 13 through 16. The order in which the flip-flops are connected to the Digiswitch is merely inverted. By use of the information in figure 46 and the fact that terminal \( c \) is to go to 0 volts only if the desired number is present in the register, the connections for the rest of the Digiswitch terminals is determined and is shown in figures 47 through 50. The "tens" dial is connected to the second group of four register flip-flops 5 through 8. In the "reverse" position flip-flops 9 through 12 are connected. The "hundreds" dial is connected to the third group of four flip-flops 9 through 12. In the "reverse" position flip-flops 5 through 8 are connected. The "thousands" dial is connected to the last four group of flip-flops 13 through 16. In the
Figure 47. Interconnections of Digiswitch "units" dial, "forward and reverse" switch, and register.
Figure 48. Interconnections of Digiswitch "tens" dial, "Forward and reverse" switch, and register.
Figure 49. Interconnections of Digiswitch "hundreds" dial, "forward and reverse" switch, and register.
Figure 50. Interconnections of Digiswitch "thousands" dial, "forward and reverse" switch, and register.
"reverse" position flip-flops 1 through 4 are connected.

Gate 15, the "decoder" gate is shown in figure 51. Three conditions are necessary for the transistor to cut off. First, gate 14 must sense that a word is present in the register. When this condition is met, input 1 of the "decoder" gate is held at 0 volts by gate 14. Second, the desired word must be present in the register. When this condition is met, terminals c of the Digiswitch hold input 2 at 0 volts. Third, the last bit of the incoming code word must return to 0 volts thereby completing the code word. When this condition is met, point C2 of the "0" level detector holds input 3 at -1 volt. Under the three above conditions the base of the "decoder" gate transistor goes positive and the transistor cuts off. A minimum beta of 88 is required to saturate the transistor.

When the correct word has been decoded, the output voltage of the "decoder" gate activates gate 16, the relay driver shown in figure 52. The relay used was a Zettler model AZ420 with a resistance of 700 ohms. When the collector of the relay driver transistor is clamped to 0 volts by the output voltage of the "decoder" gate, 21 milliamps flows through the relay coil. It is seen that the relay driver transistor also clamps point c of the input amplifier to ground to prevent the entry of any further code word bits so that the register will not shift. The input amplifier will supply a maximum additional current of 1.37 milliamps into the collector of the relay driver transistor. Point d of univibrator number 4 is also clamped to ground by the relay driver transistor and will supply an additional current of 1.4 milliamps. A maximum current of 23.77 milliamps can flow into the collector of the relay driver transistor.
Figure 51. Gate 15, the "decoder" gate.

Figure 52. Gate 16, the relay driver.
A minimum beta of 98 is required to saturate this transistor under the above conditions. Capacitor $C_1$ functions as a speed-up capacitor. The collector of the transistor is clamped to 0 volts in 10 microseconds. Diode $D_1$ supplies a path for the relay coil current when the transistor cuts off. The closing of the relay may be used for other desired functions such as initiating the copying of the data of the coded tape onto other tapes at the signal of a selected code word.
RESULTS AND CONCLUSIONS

A prototype model of the magnetic tape coder and decoder was constructed and tested. Front and rear views of the prototype are shown in figure 53. The unit generated code words up to a maximum speed of 1000 words per second. The code word bit generation occurred at a maximum frequency of 25,000 cycles per second. Code words were recorded on a Precision Instrument and an Ampex 300 frequency modulated tape recorder. The maximum tape speed available was 15 inches per second. The upper frequency response at this speed was 2000 cycles per second. The decoding circuitry was tested at a frequency of 1000 cycles per second and operated satisfactorily. The unit functioned successfully according to its intended purpose. The generated code was both visually recognizable and electronically detectable.

Some possible improvements may be incorporated into future models of the system. For example, it was noticed that one recording track was used to record the code words. Perhaps it would be possible to superimpose the code words onto one of the data tracks which records very low-frequency data. The data could then be filtered out prior to the decoding and only the higher frequency code words would cause the decoding circuitry to operate. The code words would still be visually recognizable on a pen recording of the data. Some form of error correcting or detecting scheme may also be formulated in future models.
Figure 53. Front and rear views of the magnetic tape coder and decoder prototype.
BIBLIOGRAPHY


