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Resistive Switching in SiO\textsubscript{x}-Based Systems

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ABSTRACT

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Voltage-controlled resistive switching in various gap systems on SiO$_2$ substrates is demonstrated. The nanosized gaps are made by several means using different materials including metals, semiconductors and amorphous carbon. The switching site is further reduced in size by using multi-walled carbon nanotubes and single-walled carbon nanotubes. The switching in all the gap systems shares the same characteristics. This independence of switching on the material compositions of the electrodes, accompanied by observable damage to the SiO$_2$ substrate at the gap region, bespeaks the intrinsic switching from post-breakdown SiO$_2$. It calls for caution when studying resistive switching in nanosystems on oxide substrates, since oxide breakdown extrinsic to the nanosystem can mimic resistive switching. Meanwhile, the devices show promising memory properties. The observed intermediate states reveal the filamentary nature of the switching. The switching is further explored in a vertical representation as potential candidate for high-density memory applications.
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1. Introductions & Background

1.1 Why Pursue Resistance-Change Memory?

The ever-increasing demand in portable electronic devices has made the flash memory the fastest-growing type of memory\(^1\) (see Fig. 1). Some even predicted that flash memory would replace hard disk in some ultra-light notebook or tablet computers.\(^2\) Nevertheless, a miniaturization limit is projected as the industry moves toward memory cells with 22-nm lateral width in 2016.\(^3,4\) The main reason is that, for a charge-storage based memory, it becomes increasingly difficult to reliably control or retain electrons in the shrinking dimensions.\(^3\) Although new technology such as multilevel cell (MLC)\(^2\) eases the problem to a point, common challenges such as short-channel effects or gate tunneling remain.\(^1\)

![Figure 1. Memory Market Trend (Revenue Based) (Source: Dataquest, Semico, iSuppli, Samsung).](image)

Regarding the limit in conventional device scaling (e.g., simply making the transistor smaller), various concepts and studies in fields such as molecular
electronics,\textsuperscript{5-8} spintronics\textsuperscript{9-11} have been brought about and pursued as potential replacements. One of the promising candidates is resistive switching memory\textsuperscript{12,13} based on resistance-change materials (RCMs),\textsuperscript{3} in which the RCM is usually sandwiched between two electrodes, serving as the basic memory unit (see Fig. 2a for illustration). During the programming process, electrical stress (voltage) is applied on the RCM between the two electrodes. The conductance of the RCM can be altered according to the amount of electrical stress applied. The change of the conductance is usually larger than 1000\%, with the RCM retaining its conductance even when it is unbiased. Therefore, a memory unit in a two-terminal configuration, instead of a three-terminal one adopted in transistor in conventional flash memory, can be constructed. For example, the low-conductance (OFF) and high-conductance (ON) states can be read as binary states of “0” and “1” for data storage. For addressable memory arrays, a crossbar structure (in conjunction with diodes) is usually adopted (see Fig. 2b).

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig2.png}
\caption{(a). Illustration of RCM material sandwiched between two electrodes as the basic memory unit, in which electrical stress (voltage or current) is applied between two electrodes. (b). A schematic of memory array based on crossbar structure (a diode is needed for each memory unit at one of the RCM/electrode interfaces, but is not shown in this here). Graphics are reproductions from Ref. [12].}
\end{figure}
Compared to flash memory, RCM memory features the following advantages: (1) It is non charge-based. Both phase-change and programmable metallization memories (will discuss later) seem to promise a much extended scaling without losing the device functionality. For example, in programmable metallization memory, researchers demonstrated that a metallic bridge can be scaled controllably down to 0.5 nm.\(^{14}\) (2). Simpler structure. The two-terminal configuration enables simpler memory architecture. In other words, it takes up less space and fabrication cost to construct the same number of memory units, indicating higher memory density and lower storage price. The two-terminal resistor-like structure in a way promises an easier multilevel-stacking scheme to construct real 3-D memory.\(^{13}\) (3). Fast switching time. The process of charge-and-discharge through a gate oxide in flash memory limits the switching time to above microsecond. The switching in RCMs can be down to several nanoseconds,\(^{3,15}\) making it a much faster memory.

Despite of the above promising features for nonvolatile memory, RCM memories also have certain disadvantages: (1). Reliability concern. For flash memory, a minimum memory endurance (memory cycles) of \(10^4\) and data storage time of \(\sim 10\) years are usually met. Although memory cycles as high as \(10^6\) have been demonstrated in some literature,\(^{16}\) with an extrapolated data retention time over 10 years,\(^{17-19}\) no sufficient data is provided in device uniformity (device yield and variations).\(^ {12}\) (b). Power consumption concerns. The programming current in a float-gate memory unit in flash memory is below nanoampere (nA) since the current
is mainly a tunneling current through the SiO₂ layer to charge/discharge the unit. For most RCM memories, this current is above microampere (μA). The high programming current counteracts the fast switching time as power consumption is proportional to the product of both. While optimization in architecture or software can ease the problem of comparatively slow programming in flash memory to achieve higher speed, no such rule could be applied when comes to power consumption, from which heat dissipation will in turn prevent memory density.

These pros and cons have stimulated a great interest in this field since 1960s and more efforts are likely to be put into it given the huge economic stake involved (e.g., the memory market in 2007 is $60 billion with flash memory representing a third of it). On the other hand, the switching mechanisms in various RCMs are also related to basic understandings involving physics, chemistry and material science, which are still yet to explore.

1.2 Classification of RCMs

1.2-1 Classification based on phenomenal behavior

Usually, RCMs can be categorized from two aspects. The first aspect is phenomenological behavior or current-voltage (I-V) evolutions. On the basis of I-V characteristics, the switching in RCMs is either unipolar (nonpolar) or bipolar.

In unipolar switching, the change of the resistance depends on the amplitude of
applied voltage but not on the polarity (e.g., whether it is positively or negatively biased). Because of the nonpolarity dependence, the switching is likely to be Joule heating related. In the electroformed device (most pristine RCMs are insulating or semiconducting; high voltage is needed to initialize the RCMs into switching states, which is referred to as electroforming process), as shown by green and grey curves in Fig. 3a, the ON state can be changed into an OFF state by sweeping to a certain voltage (threshold “reset” voltage). As shown by the red curves in Fig. 3b, the change from an OFF state back to an ON state involves another threshold voltage (“set” voltage). Since the reset process (from ON to OFF) is likely to be Joule-heat-related breaking of the conducting paths, a current compliance (CC) is usually needed for the set process (indicated by the red dashed curves in Fig. 3a). These two processes are symmetric in both positive and negative voltage bias regions as shown in Fig. 3a. By applying voltages (pulses) of different amplitudes, for example, at the set/reset threshold voltage, the conduction (memory) state of the material can be “written”/“erased” to be corresponding ON/OFF state. Usually this type of switching is observed in highly insulating oxides, such as NiO, Al$_2$O$_3$, ZnO, ZrO, and SiO, with the set voltage value not necessarily larger than the reset one.
In the other type of bipolar switching, the change of resistance is polarity dependent. Usually a threshold voltage value in a given polarity sets the material from an OFF state into an ON state (see left side in illustration in Fig. 3b), whereas a threshold voltage value (not necessarily having the same amplitudes) in the opposite polarity reset the ON state into OFF state (see right side in Fig. 3b). This type of switching behavior is usually observed in semiconducting oxides, such as complex perovskite oxides. Some materials, such as TiO$_2$, Cu-doped SiO$_2$ can show both unipolar and bipolar switching behaviors.

1.2-2 Classification based on mechanism.

Based on the switching mechanism, RCM based memory can be categorized as (i) phase-change memory, (ii) programmable-metallization (metal-filament based) memory (iii) metal-oxide (oxygen-vacancy based) memory.
Phase-change memory relies on a resistance change between the ordered crystalline state and a disordered amorphous form\(^3,31\) (see left images in Fig. 4 as illustration). The transition of these two states is triggered by electrical heating through applied voltage bias. Depending on the amplitude and duration of the electrical signal applied, the material can solidify into a crystalline low-resistance state or into an amorphous high-resistance state. For example, in Ge\(_2\)Sb\(_2\)Te\(_5\), a pulse heating (~10 ns) above the melting temperature (~600 °C) with subsequent rapid cooling (~10\(^9\) K s\(^{-1}\)) can amorphize the material, while a longer heating (e.g., 100 ns) below the melting temperature can recrystallize it.\(^32\) A majority of phase-change materials fall into the chalcogenides such as Ge\(_2\)Sb\(_2\)Te\(_5\), GeTe,\(^33\) and SbTe.\(^34\)

Programmable metallization memory is based on mobile metal ions embedded in a solid electrolyte glass matrix\(^3\) (see middle images in Fig. 4 as illustration). Usually an electrochemical process of reduction-oxidization (redox) of metal ions is believed to be responsible for the switching, in which the creation or annihilation of a nanoscale metallic conducting path (metal filament) results in the ON or OFF state. Since the electrochemical redox process is polarity dependent, this type of memory usually has a bipolar switching behavior. Included in this category are metal doped systems\(^13\) such as Ag\(_2\)S,\(^35\) CuS,\(^36\) Cu-doped SiO\(_2\).\(^30\)
Oxygen vacancies are considered to be the responsible cause in resistive switching observed in various transition-metal oxides, ranging from perovskites such as SrTiO$_3$ to binary oxides such as NiO. Although not yet fully understood, the movement of oxygen vacancies (particularly at the vicinity of the electrode/material interface [12]) modulates the valence of the transition-metal ions (e.g., between Ti$^{3+}$ and Ti$^{4+}$ in TiO$_2$) and thus the conducting state$^3$ (see right images in Figure 4 as illustration). Studies$^{13,37}$ showed that this type switching is similar to programmable metallization memory in that the switching is largely through filamentary conduction.

1.3 Resistive switching in low-dimension nanomaterials

Strictly speaking, modern electronics are mostly based on structures at or
approaching nanoscale. As mentioned above, one of the advantages of RCMs is indeed the promise of extended scaling down to sub 100 nm. At this scale, any of the RCM structures fabricated by standard lithographic technology could be considered as nanomaterials. However, to a point, nature has the preference of assembling small structures from bottom-up, which a top-down method may even not be able to reproduce. Among them, materials such as fullerenes, carbon nanotubes (CNTs) are perfect examples which are even considered as new carbon forms. The self-constricted and highly-ordered crystalline structures make them always be referred as 0-D or 1-D systems. In a similar way, various nanowires grown from bottom-up, though often not as perfect as fullerenes or CNTs in regard of the crystalline structure particularly at the surface region, could also be considered as quasi-1D structures due to the high aspect ration between its length and diameter. The discovery of graphene (single, or few layers of graphite sheets), on the other hand, leads to strictly defined 2-D materials.

Those quasi 1-D or 2-D nanomaterials, for the small but highly-ordered structures, have been studied to show new/enhanced functions and serve as proof-of-concepts for future device miniaturization. For example, semiconducting single-walled carbon nanotubes (SWCNTs), with the diameters ~ 2 nm, have been studied to show transistor properties exceeding those of current Si transistor in some aspects. Similarly, two-terminal memory effects in those nanomaterials have also been found and studied in the hope of potential future applications. On the other hand, the constriction in at least one dimension in those materials is likely to facilitate an easier observation of the memory switching events, thus helps to elucidate the mechanism. Followings are three recent examples of resistive switching in quasi 1-D
or 2-D materials.

Shown in Fig. 5 is one example that researchers found memory switching behavior in graphene layers.\textsuperscript{47} Initially, the graphene was patterned between two electrodes on a SiO\textsubscript{2} substrate (see Fig. 5a left image). Then by voltage sweeping to a high value, electrical breakdown in the graphene layer was induced and a gap feature was produced (see right image in Fig. 5a, indicated by two red arrows). Using voltage pulses of different amplitudes of +4 V and +6 V, memory states of ON and OFF can be programmed, respectively (see Fig. 5b). Open-and-break motions in carbon-carbon bonds at the gap region were proposed to be the mechanism (see illustration in Fig. 5c).

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure5.png}
\caption{(a). (left) as-made graphene device and (right) a magnified image after electrical breakdown in the graphene sheet, showing gap feature (indicated by red arrows). (b). Memory programming (cycles) using +4 V and +6 V pulses as writing and erasing voltages, respectively. (c). A schematic of ON/OFF state produced by forming/breaking a carbon-carbon bond. Graphics are reproductions from...}
\end{figure}
Shown in Fig. 6 is another example showing memory effect in GeTe nanowires (see inset in Fig. 6a) encapsulated by SiO$_2$ (20 nm thickness). Changes in a void structure were observed during different conduction states (see Fig. 6a and b) and were proposed to be responsible for the memory switching in the phase-change material of GeTe. The programming process is similar to that in the graphene device described above, by using voltage pulses of +5 V and +10 V, the nanowire device could be programmed into an ON and OFF state, respectively. The achieved ON/OFF ratio (~$10^7$), however, is a way higher compared to the values observed in phase-change materials; and the programming process (e.g., amplitudes of programming voltages) is also different.

Figure 6. (a), an I-V evolution in a GeTe nanowire encapsulated by SiO$_2$ outer shell, with the Inset shows the actual device patterned between two electrodes. (b). A serials of void evolutions with each number corresponding to that indicated in the IV curves in (a). Graphics are reproductions from Ref. [48].
Tour's group at Rice University also found resistive switching in nanocable structure, in which the nanocable is a SiO$_2$ nanowire coated with graphitic layer by chemical vapor deposition (CVD). By voltage sweep to a high value to induce an electrical breakdown in the outer graphitic shell to produce a gap region (see Fig. 7a), memory switching can be induced. Again, the switching behavior is similar to that in the previous two systems: by using a set of voltage pulses of +4 V and +8 V, the nanocable can be programmed into an ON and OFF state, respectively (see Fig. 7b). Electromechanical open-and-break motions of the graphitic layer at the gap region were proposed to be the underlying cause (see Fig. 7c for illustration).

![Figure 7](image_url)

**Figure 7.** (a) An electrical-breakdown nanocable, showing gap feature in the outer graphitic shell. (b). Memory cycles (programming) using +4 V and +8 V as writing and erasing voltages, respectively. (c). A proposed mechanism showing open-and-break motions of the graphitic sheets at the gap region. Graphics are reproductions from Ref. [49].

Albeit very different in material compositions and structures, the above resistive
switching systems share the similarities in: (1) Gap/void features: a gap (e.g., in graphene and nanocable switching systems) or void region (e.g., in GeTe nanowire) was observed in the conducting layer. (2) SiO₂ as insulating layer: SiO₂ was used as substrate (e.g. in graphene), supporting core (e.g., in nanocable), and encapsulating shell (e.g., in GeTe nanowire). (3) Switching behaviors: in all the above devices, a medium voltage (e.g., between 3-5 V) was used for a writing operation (i.e., set the state from OFF to ON) while a higher voltage (e.g., 6-10 V) was used for an erasing operation (i.e., set the state from ON to OFF). For the insulating property of SiO₂, it is easily to attribute all the conduction to the conducting material itself. Consequently, the direct observation of gap/void regions in these systems leads to the conclusions that touch-and-detach motions of the two broken ends of the conducting material are the cause for the ON-and-OFF switches.

However, a local high electrical field is built up during programming at the gap/void region, which was largely neglected. Take the nanocable for example. The width of the gap is ~ 10 nm (see Fig. 7a). During an erasing operation using a +8 V to set the device from ON to OFF, the voltage mainly drops at the gap region once an OFF state is obtained. A rough estimate of the local electrical field is 8V/10 nm or 8MV/cm, which is a very large value close to the breakdown value of most SiO₂, even that there may be some region having the width smaller than 10 nm. Will anything then happen to the SiO₂ layer in the gap region and contribute to the switching?
2. Thesis Main

2.1 Resistive Switching in Nanogap Systems on SiO$_2$ substrates

Therefore, it is of significance to carry out the study of local field effect on the resistive switching in similar nanosystems, in particular, to clarify whether it is safe to attribute the switching to the material without concern from the substrates. In this part, voltage-controlled resistive switching is demonstrated in various gap systems on SiO$_2$ substrates. The nanosized gaps are made by several means using different materials including metals, semiconductors and amorphous carbon. The switching site is further reduced in size by using multi-walled carbon nanotubes and single-walled carbon nanotubes. The switching in all the gap systems shares the same characteristics. This independence of switching on the material compositions of the electrodes, accompanied by observable damage to the SiO$_2$ substrate at the gap region, bespeaks the intrinsic switching from post-breakdown SiO$_2$. It calls for caution when studying resistive switching in nanosystems on oxide substrates, since oxide breakdown extrinsic to the nanosystem can mimic resistive switching. Meanwhile, the high ON/OFF ratio ($\sim10^5$), fast switching time (2 $\mu$s, tested limit), and durable cycles show promising memory properties. The observed intermediate states reveal the filamentary nature of the switching.

2.1-1 Resistive Switching in Metal-Metal Nanogaps$^{52}$

Shown in Fig. 8a is a metal-metal nanogap system by a pair of tungsten (W) electrodes separated by $\sim$50 nm on a thermal-oxidized Si surface (the SiO$_2$ thickness
is 200 nm, and the same thickness is used for all the following devices), defined by a
standard electron beam lithography (EBL) and lift-off process. Electrical
characterizations were performed using an Agilent 4155C semiconductor parameter
analyzer and a data acquisition system (NI USB-6251 BNC) in a vacuum environment
($\sim 10^{-5}$ Torr).

Bias voltage was applied between the two electrodes by sweeping from 0 V to 30
V and then back to 0 V (Fig. 8b). The device shows no conduction during the initial
forward sweep from 0 V to 25 V (e.g., the current is at the noise level, $\sim 10^{-12}$ A, of the
instrument). Substantial conduction begins at $\sim 25$ V with a sudden current increase at
$\sim 30$ V, indicating a SiO$_2$ BD. An irreversible resistance change takes place in the
post-BD device, indicated by the increased current level during the subsequent
backward sweep from 30 V to $\sim 6$ V. The sudden current (or conductance) rise at $\sim 6$ V
(indicated by the red arrow in Fig. 8b) in this backward sweep indicates the initiation
of hysteretic current-voltage curves ($I$-$V$s) essential for memory switching. Fig. 8c
shows the two characteristic $I$-$V$s of the post-BD device: in a forward sweep (0 V $\rightarrow$
10 V, blue curve), beginning with an OFF state, the device jumps to an ON state at
$\sim 3.5$ V and goes back to OFF at $\sim 5$ V. In the backward sweep (10 V $\rightarrow$ 0 V, red curve),
it jumps from an OFF state to an ON state at $\sim 5$ V and keeps the ON state below 5 V.
(Note: A fast voltage drop edge$^{20}$ is expected at the end of each forward sweep, which
sets the device state. So the beginning conduction state for a forward sweep is
determined by the previous forward sweep. Here the characteristic forward $I$-$V$ was
obtained after at least another forward sweep prior to it in the same voltage range. So it begins with an OFF state. All the following characteristic forward $I$-$V$s were obtained in this way, unless otherwise specified.) Consequently, a current hysteresis is produced in the bias range below 3.5 V (region "I" in Fig. 8c). The underlying information about the two $I$-$V$s is that a fast voltage drop edge above 3.5 V (region "II" in Fig. 8c) can set the conductance of the device into a value corresponding to the set voltage.\textsuperscript{20} For example, a +4 V (2 μs, instrumentation limit) pulse "writes" the device into an ON state, while a +10 V pulse "erases" the device to an OFF state. The set states can be read out in the lower bias region I without being destroyed, demonstrating the non-destructive memory property. Fig. 8d shows the corresponding memory cycles in the device, with an ON/OFF ratio close to $10^5$. 
Figure 8. (a). Schematic of the W-W gap and the SEM image. (b). $I-V$ of the initial sweep from $0 \text{ V} \rightarrow 30 \text{ V} \rightarrow 0 \text{ V}$ in the as-made 50nm-gap device. (c). $I-V$s of a forward ($0 \text{ V} \rightarrow 10 \text{ V}$, blue curve) and subsequent backward ($10 \text{ V} \rightarrow 0 \text{ V}$, red curve) in the electroformed device. The black dashed vertical line separates region "I" (reading) and region "II" (writing/erasing). The inset shows the $I-V$s in region "I" using an $I-V^{1/2}$ plot. (d). Memory cycles of the device: after every five readings at $+1 \text{ V}$, the device was set by an erasing pulse $+10 \text{ V}$ or a writing pulse $+4 \text{ V}$. The top panel shows the corresponding pulses. (e). $I-V$s in three as-made devices with W-W spacing of 30 nm (green curve), 50 nm (dark green curve), and 70 nm (black curve). The pictures beside each curve show the corresponding SEM images of the devices, with the red scale bars 100 nm in length.

The SiO$_2$ BD induced conduction is supported by the linear dependence of BD
threshold voltage on the electrode-electrode spacing. Gap spacing of \(-30\), \(-50\), and \(-70\) nm result in BD threshold values of \(-18\) V, \(-29\) V, and \(-39\) V, respectively (Fig. 8e). The corresponding averaged electric field is \(-6\) MV/cm, which falls into the typical BD values of SiO$_2$.\textsuperscript{51} The surface region is also expected to induce BD more easily than bulk given the higher likely density of defects. The sudden current increase during the first sweep is accompanied by observable SiO$_2$ substrate damage in the gap region. Subsequent forward or backward sweeps usually undergo gradual current increases and fluctuations having the characteristics increasingly like those of the forward or backward I-Vs depicted in Fig. 8c. This electroforming process resembles that observed in vertical M/SiO/M ("M" denotes conducting electrodes) switching systems,\textsuperscript{20} in which the amorphous form of SiO is the conducting and switching medium. The non-ohmic I-Vs, both for ON and OFF states, are dominated by Poole-Frenkel conduction having the characteristic of \(\log(I) \propto V^{1/2}\) (inset in Fig. 8c). Using the Poole-Frenkel expression\textsuperscript{53} \(I = I_0 \exp\left(\frac{\beta_{PF} E^{1/2}}{kT}\right)\) for fitting (\(k\) is the Boltzmann constant, \(T\) the temperature, and \(E\) the electric field; here \(T\) is at room temperature 300 K and the gap width \(d = 50\) nm \((E=V/d)\)), we obtain a Poole-Frenkel field-lowering coefficient \(\beta_{PF} = 3.4 \times 10^{-5} e V m^{1/2} V^{-1/2}\)) from the OFF state is very close to the theoretical one of \(\beta_{PF} = 3.8 \times 10^{-5} e V m^{1/2} V^{-1/2}\) and other experimental values in SiO$_x$.\textsuperscript{53}

2.1-2 Resistive Switching in Nanogaps by Electrical BD in Conducting Films

Argument would arise in the above representation of a pair of bare metal
electrodes on SiO₂, as metal filament (conduction through metal migration from the
two electrodes at high electric field) is always the first thought to catch. One way to
get rid of metal effect is to use nonmetal electrodes. The electric field assisted BD in
conducting materials⁴⁷,⁴⁹,⁵⁴,⁵⁵ offers another means for nanogap generation in
nonmetal films. A lift-off process was used to define an amorphous carbon (α-C)
stripe (~ 40 nm thick, by sputtering from a carbon graphite target) on a SiO₂ substrate.
Two platinum (Pt) electrodes, with a comparatively large spacing (~0.8 μm), were
then defined (see top inset in Fig. 9a). A 5-min annealing at 600 °C in Ar/H₂
environment (Ar and H₂ flow rates are 450 sccm and 150 sccm, respectively) was
performed to improve the conductivities of both α-C layer and contacts. Bias voltage
was applied between the two electrodes. The sudden current drop at ~5.8 V (Fig. 9a)
indicates a BD in the α-C stripe. A scanning electron microscope (SEM) image
reveals a cracked region perpendicular to the current direction in the α-C stripe (Fig.
9b). The reduced conduction immediately after the α-C BD (see the subsequent
backward sweep in bottom inset in Fig. 9a) has similar Poole-Frenkel feature to that
seen in Fig. 8c, indicating the disruption of the α-C layer and simultaneous BD in
SiO₂ in the gap region. The conductance jump at ~6 V (bottom inset in Fig. 9a) during
this backward sweep, initiates the similar electroforming process as discussed above
in the W-W gap (Fig. 8b). The characteristic forward I-V (Fig. 9c) and switching (Fig.
9d) show similar features to those in the W-W gap (Figure 8c, d) such as current
levels, writing/erasing voltages, ON/OFF ratio, and switching times (2 μs). While the
threshold BD voltage in α-C tends to be proportional to the electrode-electrode
spacing, the writing/erasing voltages for switching tend to be independent of it, consistent with the local switching nature within the gap region; since the collective resistance of the contacts and α-C layer is considerably smaller than that of the gap region, the bias voltage largely drops across the gap.

![Image](image_url)

**Figure 9.** (a). $I-V$ of the initial forward sweep in the as-made α-C device. The top inset shows the SEM image of a patterned device. The bottom inset shows the $I-V$ of the subsequent backward sweep right after α-C BD. (b). SEM image of the α-C stripe between the two Pt electrodes after the α-C BD. The red arrows indicate the BD-induced gap region. (c). The characteristic forward $I-V$ in the electroformed device. (d). Memory cycles using $+1$ V (5 reads), $+4$ V (write), and $+10$ V (erase) pulses.

Compared to the EBL-defined W-W gaps, the α-C BD-induced gap reduces the initial BD and electroforming voltage of SiO$_2$ in the gap region since the narrowest part is expected to be smaller than 30 nm. The switching behavior and evolutions are
quite similar to those observed in nanocable structures,\textsuperscript{49} in which the outer graphitic shell was grown by CVD method and much more ordered in \( \text{sp}^2 \) forms. It was because of this ordered sheet structures, electromechanical motion between individual sheets at the gap region was proposed to be the switching cause.\textsuperscript{49} A simple argument should follow that the configurations of microstructure of individual carbon sheet should affect the switching to a point. However, albeit the difference in microstructure between amorphous carbon (which has more \( \text{sp}^3 \) components and is more disordered) and CVD carbon, the switching behaviors are quite similar between the two systems.

The carbon form, on the other hand, offers a better way to investigate the details of the gap region by removing the \( \alpha \)-C layer without destruction to the SiO\(_2\) substrate. \( \alpha \)-C was removed by oxidation (750 °C in air) in the same switching device. SEM images show substantial damage to the SiO\(_2\) part corresponding to the gap region (compare Fig. 10 a and b). Further control tests were performed in devices with same \( \alpha \)-C thicknesses and electrode spacings to investigate how the damage to SiO\(_2\) forms. In one group, we performed multiple sweeps up to a voltage slightly below the \( \alpha \)-C BD threshold value (thus no gap generation, see Fig. 11a), while in the other we produced BD in the \( \alpha \)-C layer by one single sweep to a voltage above the \( \alpha \)-C BD threshold value (see Fig. 11b). After the \( \alpha \)-C removal, observable damage to the SiO\(_2\) substrate at the gap region in the second group was found, but no damage to the SiO\(_2\) substrate was found in the first group. The results reveal that: 1) the gap generation in the \( \alpha \)-C layer simultaneously induces SiO\(_2\) BD within the gap region, which is
consistent with the reduced conduction (through post-BD SiO₂) having the Poole-Frenkel feature right after the α-C BD discussed above; 2) the damage to SiO₂ is mainly through local electric-field induced BD, as opposed to local heating, since a great reduction in current local heating is expected after the disruption of α-C layer in the gap region due to the sudden current drop. We also found that extended electroforming process and switching cycles tend to have more pronounced damage to SiO₂ substrate in the gap region. These results indicate the role of SiO₂ in switching in the gap region.

Figure 10. (a) SEM image of a resistive-switching α-carbon stripe, showing gap feature (circled by red dashed curve). (b). After carbon removal, damage to the SiO₂ substrate at the gap region was found (circled by the red dashed curve).
Figure 11. (a). Multiple $I-V$ sweeps (up to 13.5 V, which is slightly lower than the threshold BD value of 14 V) in a carbon stripe without initializing BD in the carbon layer. (b). A single sweep to 15 V induces the BD in the carbon layer.

The post-BD SiO$_2$ switching nature is further emphasized by using a different material as the gap generation medium. Electrical BD in a titanium nitride (TiN) stripe on a SiO$_2$ substrate leads to similar gap structure and switching (see Fig. 12). Compared to that in $\alpha$-C stripe, the gap in a TiN stripe is usually located at the TiN-electrode interface instead of between the electrodes. The possible reason is that the Schottky barrier at the TiN-electrode interface (since TiN is semiconducting) enhances the local field and facilitates the TiN BD at that location, as opposed to an efficient C-Pt electrical contact in the $\alpha$-C stripe, where BD in $\alpha$-C is likely to happen at the least heat-dissipation region far away from both electrodes.

Figure 12. (a). SEM image of a switching TiN stripe on SiO$_2$ substrate. The red arrows indicate the gap region induced by an initial TiN BD. The inset shows the initial TiN BD $I-V$. (b). The characteristic
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forward $I-V$ in the electroformed TiN device. (c). Memory cycles using +1 V (5 reads), +4 V (write), and +7 V (erase) pulses.

2.1-3 Resistive Switching in Nanogaps Formed by Metal Islands

A gap due to electric field BD is less likely to form in metal stripes because the high current density usually melts the metal before a BD and the surface tension of liquid metal tends to form droplets, preventing a narrow and well aligned gap. However, a thin metal film tends to form discrete islands, and nanogaps may form naturally between individual islands. For this purpose, an aluminum (Al) thin film (~10 nm thick) was deposited by sputtering on SiO$_2$ between two Pt electrodes. The surface morphology of the deposited Al studied by atomic force microscope (AFM) shows discontinuous granular features (Fig. 13a). A voltage sweep was applied between the two electrodes for the as-made device. Unlike that in α-C or TiN stripes, the initial forward sweep (0 V → 20 V) shows a much lower conductance and no sudden current drop (Fig. 13b). This further indicates the discontinuity of the Al film. The subsequent backward sweep (20 V → 0 V), with a conductance jump, indicates the initiation of hysteretic behavior. The SEM image of the electroformed device shows a granular Al surface between the electrodes (Fig. 13c) with no such apparent gap (Fig. 13d) as that produced by BD in α-C or TiN stripes, which is consistent with the $I-V$ feature of the initial sweep discussed and in support of the idea of switching in as-formed island-island gaps. Although the actual switching site is unknown due to numerous indistinguishable gaps between islands, it is expected that the relatively high resistance of the Al film reduces both the current and effective voltage drop.
across the switching site. Therefore, the switching device has higher writing/erasing voltages (Fig. 13e) and lower ON current (Fig. 13f).

Figure 13. (a). AFM surface morphology of Al film between the two Pt electrodes. (b). \textit{I-V} of the initial double sweep (0 V $\rightarrow$ 20 V $\rightarrow$ 0 V, indicated by the black arrows) in the as-made Al-island device. (c). SEM image of the Al film of the switching device, showing the granular structures. (d). SEM image of the Al-island after switching, showing no apparent gap structure. (e). The characteristic \textit{I-V} of a forward sweep in the electroformed Al-island device. (f). Memory cycles using +1 V (5 reads), +6 V (write), and +14 V (erase) pulses.

2.1-4 Resistive Switching in Nanogaps Formed by Carbon Nanotubes
From the device perspective, one interesting question is, How small can the device become? Furthermore, a small and constricted switching size may offer a clearer view of the switching location, while it is relatively difficult to distinguish the actual switching site in a wide α-C stripe, e.g., whether the switching happens uniformly along the entire gap region or locally. The electrical BD in MWCNTs provides a potential means for further reduction in gap size. For this purpose, two Pt electrodes were patterned on the ends of a MWCNT (Mitsui & Co., Ltd.) with a diameter ~60 nm (Fig. 14a). Fig. 14b shows the SEM image of the pristine device. Electrical BD begins at a voltage ~5 V indicated by a sudden current drop (bottom inset in Fig. 14c). The corresponding SEM image right after this BD shows a broken gap region (Fig. 14c and top inset). The subsequent sweeps electroform the device, showing the characteristic switching $I-V$ (bottom inset in Fig. 14d) similar to those observed in all the above devices. The SEM image of the electroformed device shows clear damage to the SiO$_2$ at the gap region, extending beyond the nanotube (Fig. 14d and top inset). Note that switching in electrical BD MWCNTs was reported previously.$^{60}$ The ON and OFF states were achieved by close-and-break motion of the carbon nanotube shells from the two broken ends, and were stable up to only several cycles.$^{50}$ The switching here is attributed to the post-BD SiO$_2$ at the gap region and is stable with extended cycling (Fig. 14e). The non-mechanical switching of the nanotube itself is also supported by the high yield in our devices (e.g. 10 out of 10 MWCNT devices tested show similar switching) regardless of the actual details of the broken ends. This is in contrast to nanotube-based mechanical switching since we
expect that both the broken gap size and the morphology of the broken ends would affect the behavior.
Figure 14. (a) Schematic of two Pt electrodes patterned on a MWCNT atop a SiO₂ substrate. (b) SEM image of the as-made MWCNT device before electrical characterization. (c). SEM image of the same MWCNT immediately after BD. The bottom inset shows the BD $I$-$V$ and the top inset is a magnified view showing the gap structure at the BD region. (d). SEM image of the same MWCNT device after electroforming. The bottom inset shows the corresponding characteristic forward $I$-$V$ and the top inset is the magnified view of the gap region showing SiO₂ damage. (e). $10^3$ cycles in a second MWCNT device, with the reading, writing, and erasing pulses of +0.5 V, +3.5 V, and +6 V, respectively.

Single-walled carbon nanotubes (SWCNTs) are candidates for ultra-small constrictions. Electrical BD in metallic SWCNTs was reported and used as a means for sorting semiconducting SWCNTs.⁶¹ Ti/Pt electrodes were patterned on a metallic SWCNT with a diameter ~2 nm. Electrical BD takes place at ~8.5 V (Fig. 15a). Fig. 15b, c show the characteristic $I$-$V$ and switching after BD and electroforming. The AFM image of the electroformed device shows the broken region in the SWCNT (Fig. 15d). The corresponding SEM image in Fig. 15e shows a dark dot at the gap region, indicating hole-like damage to the SiO₂ substrate, which is also inferred from the AFM image. The comparatively small ON current (Fig. 15c) in the SWCNT device is mainly attributed to the contact resistance between the broken nanotube ends and the post-BD SiO₂ in the gap region, as a good electric contact to metallic SWCNTs with diameters below 2 nm usually requires specific metals.⁶² This contact resistance also reduces the effective voltage drop across the gap, resulting in higher writing/erasing voltages (Fig. 15b).
In this SWCNT switching case, the argument of electromechanical mechanism becomes weak: with a diameter of ~2 nm for the SWCNT, how could the two broken ends stretch and retract reliably and repeatedly across a gap over 10 nm to form ON and OFF states? As a matter of fact, the above nanogap devices share the similarities once operational, regardless of the (effective) electrode compositions. These include...
similar writing/erasing voltages and currents (the reduced ON currents and increased writing/erasing voltages in Al-island and SWCNT devices are due to high film or contact resistances), switching times, and noise distributions. The comparatively large current fluctuation in the erasing bias region observed in all the devices is another characteristic of SiO$_x$ conduction.\textsuperscript{20} The approximate independence of switching on the (effective) electrode materials ranging from metals (W, Al), conducting nonmetal (C), semiconductor (TiN), to carbon nanotubes, along with the electroforming processes and observable damage to the SiO$_2$ substrate in the gap regions, bespeaks the intrinsic post-BD SiO$_2$ switching nature. This is confirmed by making similar α-C stripe structures on Si$_3$N$_4$ substrates, in which switching was not observed after the gap generation; severe substrate damage is usually observed in the gap region following an attempt of electroforming.

Common features observed in all the above devices are the various intermediate conduction states. As shown in Fig. 16a, for an initially established MWCNT-based device, characteristic forward (0 → 7 V) $I$-$V$ (green curve), an OFF state with a current level of $\sim 10^{-6}$ A can be set by a +7 V pulse (see cycles in the left column in Fig. 16b). By sweeping to a higher voltage above 7 V (black crossed curve), a lower conduction state appears, indicated by a sudden current drop at $\sim 7.5$ V (see black arrow). In the subsequent sweep, a new $I$-$V$ featuring a lower OFF state is established (see blue curve), and the same +7 V pulse now sets the OFF state to a current level of $\sim 10^{-8}$ A (see cycles in the middle column in Fig. 16b). The OFF current can be further
reduced by sweeping to an even higher voltage (see magenta crossed curve) during which a second conduction reduction appears at \(~12\) V (magenta arrow). This leads to a third \(I-V\) (cyan curve) with an OFF current level of \(\sim10^{-10}\) A that can be set by the same erasing pulse of \(+7\) V (see cycles in the right column in Fig. 16b). Multiple intermediate conduction states are an indication of filamentary conduction in oxides,\(^63\) in which different states can be viewed as formation/termination of new/existing percolation paths.\(^63\)\(^64\) To an extent, the current fluctuations in the erasing region (see cyan curve in Fig. 16a) can be viewed as various meta-stable states, e.g., same erasing voltages can produce different OFF currents if they encounter current fluctuations of different magnitudes. This is well-reflected in the \(10^3\) cycles of the MWCNT device, in which the OFF states undergo various conductance states (Fig. 14e). We attribute this to be the main cause of instability in the current device performance.

*Figure 16.* (a). \(I-V\) evolutions in an electroformed MWCNT device. Starting from an initially established forward \(I-V\) (0 V \(\rightarrow\) 7 V, green curve), the subsequent forward sweep (black crossed curve) up to a higher voltage (0 V \(\rightarrow\) 9 V) lowers the OFF state (see black arrow at \(~7.5\) V). A new characteristic forward \(I-V\) with a lower OFF state is established subsequently (blue curve). By sweeping to an even higher voltage (magenta crossed curve), a second conductance reduction in the OFF state is initiated (see magenta arrow at \(~12\) V). Similarly, a third characteristic \(I-V\) featuring even a
lower OFF state establishes thereafter (cyan curve). (b). Memory cycles using the same set of +1 V (5 reads), +3.5 V (write), and +7 V (erase) pulses in the same device, with the left, middle and right columns corresponding to the established green, blue, and cyan characteristic $I-V$ curves in (a).

2.1-5 Summary

In summary, we have demonstrated reproducible memory switching in various nanogap systems on SiO$_2$ substrates. The lack of dependence of the switching behaviors on electrode materials points to a common mechanism, post-BD SiO$_2$ switching in the gap region. It is therefore important to exercise caution when building resistive switching nanosystems on SiO$_2$ substrate. Effects should be taken to distinguish the switching cause. The high ON/OFF ratio, fast switching time, and durable cycles demonstrated here show interesting memory properties. In particular, the small switching site demonstrated in a SWCNT shows the feasibility of high-density SiO$_2$-based memory arrays if a vertical embodiment could be realized. The observed intermediate states reveal the filamentary conduction nature in post-BD SiO$_2$ switching which is likely Si-Si wire formation, although a further investigation of the individual filamentary path is needed. The post-BD SiO$_2$ conduction suggests another possible mechanistic scenario for the switching that was observed in our graphitic memories.$^{49,65}$
2.2 Resistive Switching in Vertical SiO\textsubscript{2} Structures

2.2-1 Fabrications & Switching behaviors

From a memory prospective, vertical crossbar structure is needed for high-density data storage. Topologically, the planar nanogap switching systems discussed above (see Fig. 17a for illustration) can be transferred into a vertical representation as illustrated in Fig. 17b. Furthermore, if the thickness of the SiO\textsubscript{2} layer is thin enough, e.g., close to the width of the nanogap in the planar systems, no conducting film is needed to define the nanogap, because the electrode-SiO\textsubscript{2}-electrode structure itself already defines a gap having the width of the thickness of the SiO\textsubscript{2} layer (see Fig. 17c for illustration).

![Figure 17](image)

**Figure 17.** (a) An illustration for planar nanogap systems. (b). A vertical nanogap system with conducting thin film at the vertical edges. (c). A vertical sandwiched structure of electrode-SiO\textsubscript{2}-electrode without any conducting film.

In this regard, vertical sandwiched SiO\textsubscript{2} structures were fabricated. Structures with two different oxide growth methods were examined. In the first type of structure (see Fig. 18a for illustration), SiO\textsubscript{2} with a thickness of 50 nm was grown by thermal oxidization of a silicon substrate. Then circular W electrodes (5 nm Ti was used as adhesion layer) with the diameters of 50 um and thicknesses of 100 nm were defined by photolithography and a lift-off process. Buffered oxide etch (BOE, 10:1, J. T.
Baker) was then used to remove the surrounding SiO₂, leaving the layer underneath the W electrode protected. In the second type of structure (see Fig. 18b for illustration), SiO₂ with a thickness of 50 nm was grown by plasma-enhanced chemical vapor deposition (PECVD) on a TiN/Si substrate (TiN was deposited by physical vapor deposition (PVD) on Si). 10 nm of TiN and 100 nm of W were then deposited on SiO₂ by PVD. A 70×70 μm² photoresist area was then patterned by photolithography and used as the sacrificial mask. Reactive ion etching (RIE) was used to define the vertical sandwich structures. Corresponding etching recipes (e.g., SF₆/BCl₃/Cl₂ for W etching; BCl₃/Cl₂ for TiN etching; and CF₄/CHF₃ for SiO₂ etching) were used with the layered structure underneath the photoresist protected, thereby forming the vertical structure. A several-minute annealing at 600 °C in an Ar/H₂ environment was performed before electrical characterizations. Measurements were done using an Agilent 4155C semiconductor parameter analyzer under a single sweep mode. Bias voltage was applied by a probe tip at the top W electrode with the conducting substrate grounded. All data was collected in vacuum (~10⁻² Torr) at room temperature, unless otherwise specified.
Figure 18. (a) Fabrication process of vertical devices of type 1. (b) Fabrication process of vertical devices of type 2.

Fig. 19a shows the typical $I$-$V$s in a first type of vertical W/Ti/(Thermal) SiO$_2$/Si device (DEV-1) by BOE (wet) etching under a forward (0→8 V) sweep and then a backward (8→0 V) sweep of the top electrode relative to the bottom one. The forward sweep features a high-impedance state at the low voltage region (denoted as region "I" divided by the vertical dashed line in Fig. 19a), with a sudden current jump at ~3.3 V and then a sudden drop at ~5 V into a high-impedance state again. The backward sweep, from high bias back toward 0 V, undergoes a low-impedance state at region "I". The underlying cause for this hysteretic behavior is a voltage-controlled permanent resistance change in the higher bias (writing) range (denoted as region "II" in Fig. 1a), indicated by the beginning of a sudden rise in current or conductance during the forward sweep. A rapid falling edge of voltage in this region can write the device into a conductance state corresponding to this ending voltage.\textsuperscript{20} For example, a rapid voltage drop at 4 V writes the device into an ON state, while that at 8 V erases the device into OFF (In Fig. 19a, the forward sweep was obtained after at least one forward sweep performed to the same bias range; the device had been in an OFF state since a very rapid voltage drop to 0 V, at the end of the previous forward sweep, is expected to place the device into the corresponding high-impedance state). The obtained state can be read out at the low bias region "I" without being destroyed, rendering a non-volatile memory device. In this regard, pulses as narrow as 1 μs (the
shortest pulse possible on the instrumentation) were applied to read, write and erase the device (Fig. 19b), with an ON/OFF ratio over $10^4$ achieved. The $I$-$V$s and switching behaviors obtained here are quite consistent and similar to that observed in the previous horizontal nanogap systems.

For the second type of structures of W/TiN/(PECVD) SiO$_2$/TiN/Si (DEV-2) were fabricated by RIE etching, a typical hysteresis $I$-$V$s by similar consecutive forward and backward sweeps is shown in Fig. 20a. Compared to those in Fig. 19a from the wet-etching device, the $I$-$V$s here have (1) higher ON and OFF currents and (2) comparatively smooth current changes in the writing region. The current or conductance change in this region, without a drastic rise or drop, means that the conductance state of the device can be changed semi-continuously by applying bias
pulses of different amplitudes. The color curves in Fig. 20a show how different bias sweep ranges (thus different writing voltage at the end of each forward sweep) change the conduction states of the device (again, each set of forward and backward sweeps was obtained after at least one forward sweep preformed to the same bias range). With the decreasing of the sweep range, it shows a gradual decline in the ON/OFF ratio because of an increasing current in the OFF state set by the reduced ending bias (the ON current tends to increase at a rate much smaller than that of increase in the OFF current). The writing region tends to shift toward the low bias end, indicated by the shift of the current-rise edge in the forward sweep. A multilevel or analog memory is demonstrated in Fig. 20b by applying erasing bias pulses of different amplitudes. The adjustable ON/OFF ratio is limited to up to $10^3$ due to comparatively large OFF currents.

**Figure 20.** (a). A set of $I$-$V$'s by forward and subsequent backward sweeps in DEV-2, with black (bottom), red (middle), and blue (top) curves corresponding to sweep bias ranges of 0-10, 0-8, and 0-6 V, respectively. Inset is a device schematic. (b). A series of reading the device state by applying bias pulses (1 μs) of +2 V (five reads between each set of writing-erasing pulses). The device undergoes OFF-state changes by applying erasing pulses (1 μs) of different magnitudes of +10 V, +8 V,
and +7 V (with the writing pulse +4 V unchanged) as shown correspondingly in the upper panel.

2.2-2 Switching location and mechanism discussion

To clarify where the switching takes place in these vertical devices, W or W/TiN electrodes with the same thicknesses and sizes were deposited on the (PECVD) SiO₂/TiN/Si substrate, without doing any etching of the oxide (see left schematic in Fig. 21a), or on wet-etching defined SiO₂ pillars of larger diameter on the (thermal) SiO₂/Si substrate (see right schematic in Fig. 21a). The samples were then annealed under the same conditions as those adopted for the previous structures and then characterized via electrical measurements. No conduction was observed up to a bias of 25 V ($I \sim 10^{-12}$ A). Devices with different diameters (25 μm, 50 μm, and 100 μm) were also made and the ON currents were collected for DEVs-1 and another type of wet-etching defined W/Ti/(PECVD) SiO₂/TiN/Si devices (DEVs-3, see schematic in Fig. 21b). Statistically, for both DEVs-1 and DEVs-3, the ON currents follow a trend more closely to scaling with the diameter (black dashed lines in Fig. 21d-e) than scaling with the device area (red dotted lines in Fig. 21d-e). These results reveal that the conduction (thus switching) only takes place after the etching and is localized at the vertical SiO₂ edges. On the other hand, the I-Vs of DEVs-3 tend to have some combined features of those in DEV-1 and DEV-2. For example, they typically have higher ON and OFF currents than those in DEV-1, but lower than those in DEV-2 (at the same bias sweep ranges). The forward sweep typically also begins with a sudden current rise in the writing region, but then follows a less intense declining tail. Fig.
Figure 21. (a) Schematics of devices with (left) no SiO₂ etching and (right) etched SiO₂ pillar with a smaller on-top electrode. (b) Schematic of DEV-3. (c) A set of forward sweeps starting with the OFF states in the formed vertical structures of DEV-1 (black curve), DEV-2 (blue curve), and DEV-3 (red curve). (d) ON currents at +1 V (written by 1μs, +5V pulses) for DEVs-1 and (e) ON currents at +1 V (written by 1μs, +4 V pulses) for DEVs-3, with each type having device diameters of 25 μm (rectangles), 50 μm (circles), and 100 μm (triangles). 25 data points/devices were collected for each size. The dashed black lines describe a \( I \propto D \) (diameter) scaling and the dotted red lines \( I \propto D^3 \) scaling.

The surface nature of the switching and conduction mechanisms in these vertical
structures is further emphasized by the response of devices to annealing in a reducing atmosphere. A several-minute thermal annealing at 600 °C in Ar/H₂ was necessary to observe the switching in vertical devices produced by wet etching. Before annealing, a majority (over 80%) of the devices was non-conducting (e.g., $I \approx 10^{-12}$ A at a bias up to 25V). Detectable conduction began to take place after the thermal annealing in the reducing environment. By sweeping to a high voltage (e.g., 20 V) within which some sudden current drops and large current fluctuations appeared, an electroforming process occurred. The current drops and fluctuations gradually moved toward lower bias voltages in the following sweeps, along with substantial increases in the current. Finally, reproducible forward $I-V$s as described before were established. For the devices fabricated by dry etching (DEV-2), a similar forming process can take place even before the annealing. An annealing simply obviates this forming process by introducing the device into a formed ON state for the first forward sweep.

Except for the aforementioned differences, these devices are similar in several aspects once operational. For example, they have (1) similar reading/writing bias ranges (see Fig. 3c), (2) similar noise distributions with comparatively smooth $I-V$s at the reading bias range and larger fluctuations in the writing region, and (3) fast switching time down to 1 μs. Low-temperature tests show that these devices cannot be electroformed at a temperature below 150 K, while the ON-state conductance shows relatively little temperature dependence down to 100 K. Our other tests show that the switching and forming processes in all types of the devices are bias-polarity
independent. Since all the devices are asymmetric in structure with non-metallic substrates of either Si or TiN/Si, metal filament formation is less likely to be responsible for the observed switching because such a process usually involves metal ion migration or injection from the electrode, which is bias-polarity dependent.\textsuperscript{13} Moreover, metal filaments generally have higher ON current levels than those we observed here. All the observed characteristics resemble those in the M/SiO/M system,\textsuperscript{20} where SiO plays the essential switching role. In our structures we suggest that nonstoichiometric SiO\textsubscript{x} at the edges of the etched oxide is the switching medium. While M/SiO/M systems were first studied decades ago, the detailed underlying switching mechanism remains largely unknown and debatable.\textsuperscript{20} The layered structure of SiO in the M/SiO/M system along with comparatively large and smooth currents contributed from the entire SiO layer makes it challenging to discern whether the switching is a bulk effect or is localized.

The surface-restricted switching in our system may offer new insights. As discussed before, the \textit{I-Vs} in DEVs 1-3 mainly differ in the current magnitudes and noise features. As shown in Fig. 3c, with the decreasing of the operating current level, the current fluctuations in the writing bias region increase (consider, for example, the large rises and drop in currents as the largest fluctuations). Note that in Fig. 21c the OFF current of DEV-2 is much larger than that of DEV-1, changing from a relatively smooth \textit{I-V} into one with discrete steps. We suggest that this is a consequence of having an ensemble of conducting paths in DEV-2 and only a few paths in DEV-1.
The variation in switching voltages even in the same DEV-1 by different sweeps further indicates the discrete nature of conduction paths. One can imagine that a large number of DEVs-1 in parallel would collectively reproduce the comparatively smooth $I-V$ in DEV-2 due to a variety of current rise and drop edges. The $I-V$ of DEV-3 in Fig. 21c is consistent with this idea, with an intermediate conductance device DEV-3 having features between the two limits of DEV-1 and DEV-2. These features further support discrete-path or filamentary conduction in our system at nonstoichiometric device edges, in accordance with expectations based on studies of M/SiO/M devices by different methods. And this filamentary revelation through IV behaviors is also consistent with the same conclusion indicated by intermediate states in horizontal nanogap systems (see Fig. 16). It is straightforward to expect that while a large number of filamentary paths with non-uniform writing/erasing biases would limit the overall ON/OFF ratio, reducing the path number can push this ratio up, as demonstrated in DEV-1 with an ON/OFF ratio $> 10^4$.

2.2-3 Summary

We have demonstrated reproducible resistive switching with memory properties in vertical sandwich structures with SiO$_2$ as the switching layer. The electrical characteristics depend significantly on the oxide etching method, as well as annealing history in reducing environment and oxide growth method. These traits suggest that the switching is filamentary in nature and takes place in the stoichiometrically poor edges of the etched oxide. The localized character of conducting paths and critical
role of etched oxide surfaces raise the possibility of nano-scale SiO$_x$ based memory, though an improved understanding of the detailed switching mechanism would be essential. The question of the formation of individual conduction path remains open. The heat-assisted electroforming processes in our devices and the non-working state at low temperature may indicate a fusion-and-reforming mechanism induced by local heating due to hot electrons.

2.3 On-Going & Future Work

The metallic electrodes used in the vertical memory units discussed in section 2.2 could still arise the argument about the possibility of metal filaments as the switching mechanism. On the other hand, the industry may prefer a less metal-involved process or even metal-free one. The SiO$_x$ conduction and switching nature indicates that one can use material other than metal as electrodes as long as it is conducting. A good candidate is doped polysilicon (PolySi). Fig. 22 shows the process of a metal-free fabrication of vertical SiO$_x$ memory units.
I Photoresist mask definition

II RIE dry etching of Poly-Si

Photoresist
Poly-Si
SiO\textsubscript{x}
Poly-Si

IV Electrical characterization

III SiO\textsubscript{x} etching

Figure 22. A metal-free process for PolySi-SiO\textsubscript{x}-PolySi vertical memory fabrication.

Figure 23. A memory cycle in PolySi-SiO\textsubscript{x}-PolySi vertical structure.

This PolySi-SiO\textsubscript{x}-PolySi structure shows very similar memory switching
behaviors (see Fig. 23) as those observed in previous systems. Since the elements involved in this structure are oxygen and silicon, it further confirms the SiO\(_x\) switching nature. Various tests are being carried out to understand more about its mechanism. For example, X-Ray test in which a dose of \(~50\) MRy was used, shows that the memory retains both the ON and OFF states after exposure, indicating the non charge-based nature (note that a flash memory goes bad at the dose of \(~100\) KRy). Annealing in reducing environment (Ar/H\(_2\)) would induce leakage current which could assist an initialization process. Vertical SiO\(_x\) structures with different oxygen compositions (i.e., different \(x\) values) are being made to compare the switching behaviors in order to get an optimal performance. Other tests such as reliability (memory cycles), retention time, and temperature-dependent behaviors are also being carried out or planned.

3. List of References


[36]. T. Sakamoto, H. Sunamura, H. Kawaura, T. Hasegawa, T. Nakayama, and M. Aono,


