An FPGA-based Daughtercard for TI's C6000 family of DSKs

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Abstract

In this paper we present an FPGA-based daughtercard designed for TI's C6000 family of DSP Starter Kits (DSKs). The hardware, initially designed for a course project, provides a platform for studying heterogeneous systems and hardware software co-design. Students will leverage the DSK-FPGA system for rapid prototyping of signal processing algorithms and to study task-partitioning and system integration. These techniques are becoming increasingly important for system designers as we move to system-on-chip (SoC) devices. The daughtercard hardware is fully functional, and a software package is being developed to provide a seamless communication interface between the DSK and FPGA.

1. Introduction

We present an FPGA-based daughtercard designed for Texas Instruments' C6000 family of DSP Starter Kits (DSKs) [1]. Built around a Xilinx Virtex-II Pro FPGA [2], the daughtercard together with TI's C6x DSK provides a platform for rapid prototyping of digital signal processing (DSP) algorithms using hardware-software co-design techniques. Together with the software package being developed, the platform will serve as a tool for teaching the undergraduate DSP laboratory course at Rice [3].

The paper is organized as follows. We begin with a description of our design for the daughtercard hardware. Next, we discuss the software, followed by some perspectives on the teaching benefits of the system.

2. Hardware Description

Programmability, parallelism and a widely-used, user-friendly software development environment are the key attributes that a hardware architecture must possess in order to be efficient for studying task partitioning, system integration and rapid prototyping of real-world signal processing systems. With this in mind, the daughtercard, shown in Figure 1, is built around Xilinx's Virtex-II Pro FPGA (XC2VP7). The TI DSK board provides an open interface for the design of custom extension daughtercards. Unlike the currently available FPGA-based daughtercards that are built around low-density FPGAs, our design provides enough parallel I/O and computation resources to meet the real-time requirements of complex DSP systems. The Virtex-II Pro also has an embedded PowerPC core, which together with the FPGA fabric and the C6x DSK form a platform for exploring efficient resource utilization and inter-processor communication in a heterogeneous system. Using Xilinx's ISE software [2], students will develop HDL code for targeting the FPGA. A JTAG port is provided for programming the FPGA and analyzing internal signals. The daughtercard includes user I/O, peripherals, and a debug-header providing access to 16 FPGA I/O lines. A seven-segment LED display, four LEDs, and three switches are available to display status information and signal events.

The daughtercard was designed using OrCAD Capture CIS and Allegro software tools from Cadence [4], and was hand-routed to maximize signal integrity. The daughtercard sits in the expansion slot provided by the C6x DSK and is supplied 5V and 3.3V power from the DSK board. It can also be powered by an external power supply using the jumpers and power headers provided. This supports configurations where the board may require more power than the DSK can supply, and allows the flexibility of having a larger FPGA chip in future revisions. The top-layer expansion connectors, together with the power supply design mentioned above, make it possible to have multiple daughtercards in one system. Using this feature, the I/O capabilities of the system could be expanded by stacking a daughtercard such as TI's PCM3003 stereo audio codec.

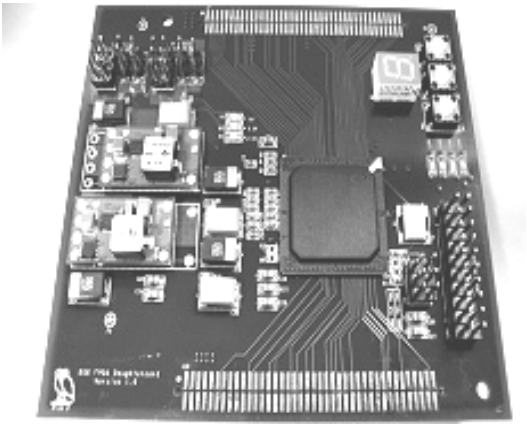

Figure 1: The Rice FPGA-based daughtercard

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The C6x DSK provides the daughtercard with access to a number of DSP and peripheral signals. These include the address and data buses for the DSP's memory, external interrupts, timer events, and data and control signals for the two multi-channel buffered serial ports (McBSP).

3. Software Design

The authors realize that good software support is essential for a hardware platform to be effectively utilized and widely deployed. A modular software package is being developed for efficient communication between the C6x DSK board and the FPGA daughtercard. The software includes C and assembly language modules for the C6x DSK and HDL code for the FPGA. This enables users to target the DSK-FPGA system without worrying about the interface, thus facilitating system-level design. Furthermore, we are currently exploring interfaces to higher-level design tools such as System Generator [2] to enhance the design process.

The interface between the C6x DSK board and the FPGA-daughtercard is shown in Figure 2. The DSK board sees the daughtercard as a memory-mapped device, and can perform data transfers using loads and stores. Additionally, the C6x DSK has a DMA engine that can provide high-throughput data transfer capabilities. The software design will use the DMA engine, load/store instructions, and external interrupts to provide a seamless communication and control interface between the C6x DSK board and FPGA daughtercard. Modules for performing interrupt-based communication and memory mapped loads and stores have already been completed. Using these modules, an adaptive FIR filter system with the DSK performing the filtering and the FPGA running the computationally more intensive coefficient update has been successfully demonstrated.

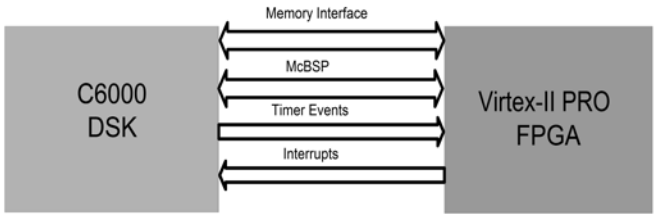

Figure 2: Interface between C6x DSK board and FPGA-based daughtercard

4. Educational Platform

Task partitioning and system integration become increasingly important as we move towards system-on-chip (SoC) structures. The DSK-FPGA architecture will help the students to better understand these concepts and explore them in a hands-on laboratory setting. Students will implement real-world DSP algorithms for tasks such as fast Fourier transform (FFT), audio reverberation, data modulation/demodulation, and digital audio filtering. Using hardware-software co-design principles, they will partition a DSP algorithm and schedule the tasks based on available resources. These exercises will help students perform complexity analysis and understand the tradeoffs involved in designing a balanced system. Leveraging the hardware platform, students will explore inter-processor communication and create mechanisms for efficient utilization of hardware resources. The availability of software modules will allow them to focus on system-level software design. Originally designed to be a companion to the C6x DSK board, we are investigating the daughtercard's use in other courses where we will be targeting the heterogeneous environment it provides. The FPGA-daughtercard, synergistic with the recent VALID initiative at Rice [5], will also help teach students FPGA design. Together with Connexions [6], an open-source e-publishing and courseware platform, the project will make system-design curriculum more accessible and interesting for students.

5. Conclusions

We have successfully developed a Xilinx Virtex-II Pro FPGA-based daughtercard for TI's C6000 DSKs. The DSK-FPGA system provides students a unique opportunity for studying task partitioning and system integration. Students will use the hardware platform and the companion software package in the DSP lab course to gain hands-on experience in rapid prototyping using hardware-software co-design.

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