REDUCING DYNAMIC POWER CONSUMPTION IN NEXT GENERATION DS-CDMA MOBILE COMMUNICATION RECEIVERS

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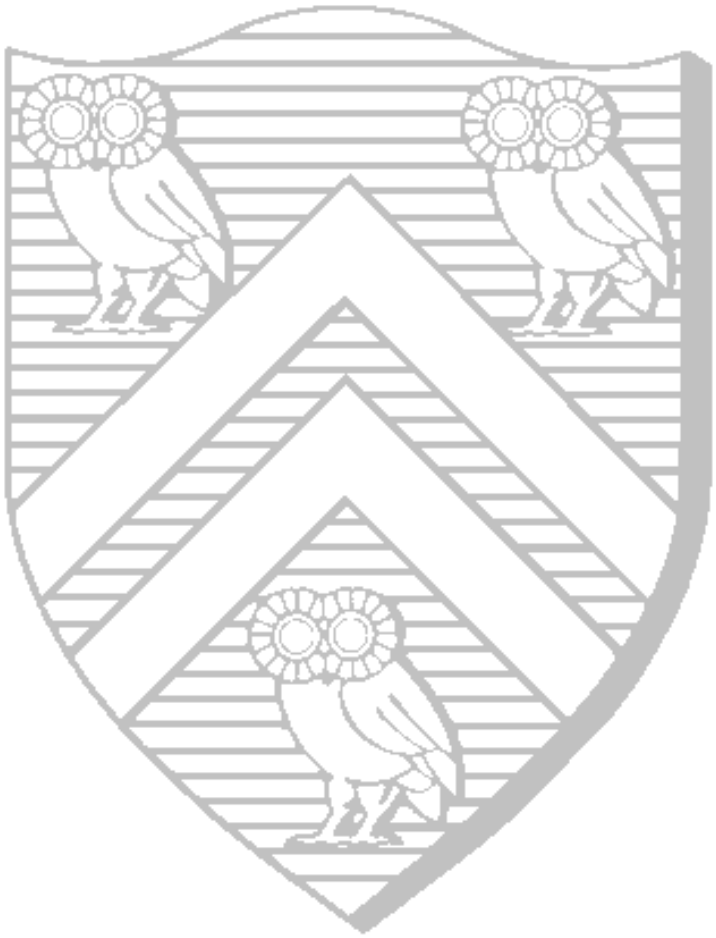

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Reducing dynamic power consumption in next generation DS-CDMA mobile communication receivers

by

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ABSTRACT

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Reduction of the power consumption in portable wireless receivers is an important consideration for next-generation cellular systems specified by standards such as the UMTS, IMT2000.

This thesis explores the design-space for reducing the dynamic power dissipation in a RAKE receiver for the Direct Sequence Code Division Multiple Access (DS-CDMA) downlink. Starting with a reference implementation of the DS-CDMA RAKE receiver, we demonstrate design methodologies for achieving significant power reduction, while highlighting the corresponding performance trade-offs. At the algorithm level, we investigate the impact of reduced precision and arithmetic complexity on the performance of the DS-CDMA RAKE receiver. We then present architectures for implementing the reference and reduced complexity DS-CDMA RAKE receivers, and analyze these architectures with respect to their dynamic power dissipation. Finally, we analyze clock-gating techniques for reducing the activity rate in both the architectures to achieve further power reduction.

Acknowledgments

If I have seen further, it is by standing on the shoulders of giants.

Sir Issac Newton

Personally, this thesis represents the culmination of a voyage of discovery in the exciting world of wireless communications system design. The work has made me understand and appreciate the amount of constraints and practical difficulties that are part and parcel of a System-on-chip (SoC) design.

My work would be incomplete without expressing my appreciation to all the people whose guidance and help made this thesis possible. I'd specially like to thank Frank Livingston for his boundless enthusiasm and willingness for spending those countless hours with me, discussing interesting ideas which formed the core behind my research. My sincere thanks to Dr. Aazhang, Ashu, Krishna Kiran and Sridhar, for answering even the most simple queries and providing me with sound technical advice. No amount of words would sufficiently convey my gratitude to my friends at Rice like Soups, Abha, Arnab, Vaya, Nasir, Aditya whose friendship added so much fun at work.

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Chapter 1

Introduction

Achieving power-efficient architectures will be a major goal in the design of next-generation mobile communication receivers such as laptops, cell phones, PDA etc. Future portable receivers will need the ability to handle various multimedia data traffic irrespective of mobility, provide guaranteed Quality-of-service (QoS) requirements, and integrate multiple functionality (GPS, World Wide Web, e-commerce etc) simultaneously. The high bandwidth required by these applications implies that these functionality would come at the expense of a heavy drain on the available battery power. Moreover, the methodologies that target power-optimized implementations will have to contend with stringent requirements for such receivers, in the form of low cost (in terms of size, weight and money), high standard of performance (in terms of standard metrics such as symbol error-rates, overcoming multi-user interference, spectral efficiency), and the ability to seamlessly transition between various standards. Shown in Table 1.1 are the specifications of a next-generation wireless standard (IMT-2000) [20]. These standards specify variable data-rates that are not only influenced by the type of data being transferred, but also by the terrain and topology of the surroundings in which the mobile is located. The high levels of expected performance, as well as the required data-rates will call for the implementation of advanced algorithms in the design of such receivers. With rapidly improving integrated-circuit (IC) technology as well as the decreasing cost of silicon area, there have been great advances in the ability to integrate the entire receiver chain on a single-chip (System-on-chip design). The point that has not been addressed in these designs is the system integration, with power minimization

Operating environment	**Terminal speed**	**Peak bit-rate**	**Target Bit-error rate**
Rural outdoor	Up to 150 mph	At least 144kbps (preferably 384 kbps)	10^{-3}-10^{-7}
Urban/suburban outdoor	Up to 90mph	At least 384 kbps (preferably 512 kbps)	10^{-3}-10^{-7}
Indoor/Low range outdoor	Up to 6 mph	2 Mbps	10^{-3}-10^{-7}

Table 1.1 : IMT-2000 Service requirements [20]

as a key constraint. The design of such architectures forms a focal point in current research in communication systems.

1.1 The Wireless channel

Fundamentally, the wireless channel is a hostile environment, characterized by mitigative phenomena such as path losses, fading, multi-path propagation delays, phase ambiguity etc. Many sophisticated transmission and reception algorithms have been proposed to combat the adverse effects of the wireless medium. A majority of these schemes exploit diversity-based techniques to improve the performance of the receivers. The diversity techniques can be classified into *temporal, frequency and spatial diversity* [22]. Temporal diversity is achieved by transmitting the same information over multiple time slots separated by at least the coherence time of the channel. This diversity also includes schemes which exploit the multi-path propagation delays of the channel, in order to obtain multiple copies of the transmitted signal that are coherently combined at the receiver. Frequency diversity exploit

a wider spectra by transferring the same information over multiple frequencies. Spatial diversity is employed by systems that transmit/receive the same transmitted signal over multiple antennae for higher performance. Such schemes have been shown to achieve a M-fold increase in the capacity where M refers to the smaller of the number of transmitter/receiver antennas [28]. What bears scrutiny will be the additional complexity incurred by these schemes which would come at the cost of higher MIPS (millions of instructions per second) requirements, if these algorithms are to be put on silicon. Once again, power-efficient implementation comes as a vital ingredient in the whole system design.

1.2 Direct Sequence Code Division Multiple Access

The DS-CDMA protocol is perhaps the most popular transmission-reception scheme employed in commercial networks today. Its principal benefits include multi-access capability (multiple users can use the channel simultaneously), protection against multipath interference, privacy, interference rejection and anti-jamming capability. In a CDMA scheme, each user is assigned a unique spreading sequence (also known as the spreading sequence or chip-sequence) for encoding the information-bearing signal. As the receiver knows the code-sequence of the user, it decodes the received signal reliably as the cross-correlations between the codes of the desired user and other users is very small. Since the bandwidth of the spreading sequence is much larger than that of the information signal, this scheme is also known as spread-spectrum multiple access [20]. Its superior performance compared to other schemes such as TDMA, FDMA etc. have made it the protocol of choice for next-generation communication transceivers. Consequently, this thesis focuses on a mobile terminal employing the DS-CDMA scheme for implementing various power-saving optimizations.

1.3 Motivation

The RAKE receiver unit forms an important constituent of a DS-CDMA mobile receiver for performing single-user detection. Essentially, it converts wide-band multi-path receiver data into a narrow-band signal which is coherently combined to generate soft/hard decisions regarding the transmitted symbols at the output. The RAKE algorithm is a conceptually simple algorithm, however, its computational complexity increases linearly with the number of multi-path components being processed. Since this algorithm is repetitively performed for detecting every information symbol, the power consumption of the corresponding implementation is an important consideration for next-generation communication receivers. With the advent of MIMO (Multiple Input Multiple Output) systems which employ multiple transmit and receiver antennas, the processing complexity of the RAKE receiver would increase linearly with the product of the number of receiver antennas and the number of multi-path components. Therefore, methodologies that discuss optimizing power consumption for the RAKE receivers now assume heightened importance.

Even though there has been considerable research investigating techniques for improving the performance of DS-CDMA RAKE receivers in fading multi-path channels, there has been comparatively little research on developing corresponding low-power receiver architectures for it. In [8], a strength reduction technique has been described for reducing the on line power dissipation in the complex RAKE multipliers by up to 25%. [16] has described power reduction techniques for a spread spectrum based correlator using a modified adder-tree structure and employing bus-invert coding. Low-power correlator architectures have been described in [26] that employ a partial correlation approach for reducing on line power dissipation during code acquisition in WCDMA based systems. To the best of our knowledge, there has been very little work on developing a unified framework which analyzes the performance vs. power dissipation trade-offs in the context of mobile DS-CDMA

RAKE receivers.

1.3.1 Contributions of the thesis

The work presented in this thesis has two principal aims. First, we analyze the impact of reduced precision and arithmetic complexity on the algorithm performance and power dissipation in the DS-CDMA mobile RAKE receiver. Next, we explore the architectural design-space for reducing the on line power dissipation. Starting with a conventional implementation of the RAKE receiver, we demonstrate design methodologies for achieving power reduction at the algorithm level and the architectural level. This "proof of concept" architecture has been implemented on a Xilinx Virtex-II FPGA and achieves the targeted data rate of 384 kbps. The resulting power-performance profiles have been obtained after passing synthesized complex receiver data simulating a urban 3 path fading channel through the targeted architectures.

- ***Algorithm level***: We show that reduction of sampling rate of the input complex multi-path receiver data to the DS-CDMA RAKE correlator during de-spreading results in favorable trade-offs in power consumption versus the corresponding receiver performance. Significant power savings are achieved through reduction in arithmetic complexity by decreasing the number of arithmetic operations during the RAKE correlation per symbol demodulation. For a 16 bit data-path, we have observed a 24.65% reduction in dynamic power dissipation in the reduced complexity RAKE receiver compared to the reference RAKE receiver implementation, with an acceptable performance loss of less than 2 dB.

- ***Architectural level***: We explore reduced precision and activity rate reduction techniques for achieving further power reduction. Starting with a 16 bit data-path, and

reducing precision till 10 bits, we study the variation in the RAKE receiver performance with decreasing fixed-point precision. We show that a 10 bit data-path approaches near floating-point performance in both the reference and reduced complexity RAKE receiver. Word-length reduction alone results in power reduction of up to 25.6% in the reference RAKE receiver architecture, and 16.96% in the reduced complexity RAKE receiver architecture. Finally, we study the effect of clock-gating based techniques for achieving activity rate reduction at the circuit level. Since operations such as Channel Estimation and Maximal Ratio Combining run at the symbol-rate, power reduction can be achieved by disabling the clock distribution for these units during their idle periods. The combined effect of reduced precision and clock-gating of idle functional units leads to significant power reduction of up to 30.5% in the reference implementation and 40.7% in the reduced complexity implementation of the DS-CDMA RAKE receiver.

1.4 Organization of the thesis

The thesis is organized as follows: The system model employed in the thesis are described in Chapter 2. Chapter 3 outlines the various aspects of the design cycle involved while transitioning from a high-level algorithm description phase to a final design implementation in the context of the RAKE receiver. Chapter 4 describes the architecture for the DS-CDMA RAKE receiver, and the individual blocks. The ensuing algorithmic and architectural optimizations for achieving power-savings are described in Chapter 5. The results of the work are presented in Chapter 6. Finally, the conclusions and future work are presented in Chapter 7.

Chapter 2

System Description

This chapter develops the system model for describing the transmission and reception of the DS-CDMA signal. Starting from a basic communication system model for highlighting the scenario (channel conditions, mobility of the user) under consideration, we discuss the transmission scheme at the base-station, the received signal model at the mobile DS-CDMA handset, and finally conclude with the description of the RAKE receiver.

2.1 Communication system model

The communication system under consideration is assumed to be formed by a single isolated circular cell of radius R with a centrally located base-station (BS). The BS communicates with the mobile users using the DS-CDMA scheme. In a macrocellular environment, the BS antennas are usually well elevated above the local terrain. No direct line-of-sight (LOS) path exists between the BS and mobile station (MS) antennas because of the natural and man-made objects that are in the immediate vicinity of the MS. As a consequence of reflections, scattering and diffraction, multiple plane waves arrive at a MS from many different directions and with different delays. This property is called multipath propagation. The multiple plane waves combine vectorially at the receiver antenna to produce a composite received signal [27]. In this thesis, we assume that the DS-CDMA mobile operates in a frequency-selective multipath fading environment with P distinct resolvable paths.

Each of these paths are characterized by the channel parameters namely

Typical Urban		**Bad Urban**	
delay, μs	Fractional Power	delay, μs	Fractional Power
0.0	0.189	0.0	0.164
0.2	0.379	0.3	0.293
0.5	0.239	1.0	0.147
1.6	0.095	1.6	0.094
2.3	0.061	5.0	0.185
5.0	0.037	6.6	0.117

Table 2.1 : Typical macrocellular urban and bad urban 6-ray power delay profiles

- $h_p(t)$: time-varying complex attenuation coefficient of the p^{th} path.
- $\tau_p(t)$: time-varying propagation delay associated with the p^{th} path.

2.1.1 Power-Delay profile

Since the mobile channel is non-stationary, the propagation delays and attenuation coefficients can change very rapidly over time. Results of the COST207 study [11, 27] for 6-ray urban and bad urban multipath delay profiles are shown in Table 2.1.

For an allowable delay spread of 1.6μs, it can be seen that

- For the typical urban environment, more than 80% of the power profile is concentrated.
- Around 60% of the power profile is concentrated within the above delay-spread for a bad urban scenario. Moreover, the strongest path component is located with a delay of 0.3μs.

The standards for third generation(3G) wireless systems such as UMTS and IMT-2000 [12] specify signalling rates up to 384 kbps for outdoor environments and 2 Mbps for local area coverage [13]. It can be inferred that the maximum delay-spread is within a symbol for outdoor and 3 symbols for indoor scenarios.

2.2 Transmission model

We consider a K user DS-CDMA downlink system employing Binary Phase Shift Keying (BPSK) symbol modulation during transmission. The k^{th} user's information sequence $b_k \in \{-1, 1\}$ is multiplied by a pseudonoise (PN) sequence whose duration equals one symbol period T_b. The generation of the PN sequence is done by a linear feedback shift register (LFSR) based arrangement. The PN sequence for the k^{th} user can be represented as a sequence of N chips each of duration T_c ($T_b = NT_c$) given by,

$$s_k(t) = \sum_{n=0}^{N-1} c_k(n) g_T(t - nT_c) \tag{2.1}$$

where $c_k(n) \in \{\frac{-1}{\sqrt{N}}, \frac{1}{\sqrt{N}}\}$ denotes the n^{th} chip and $g_T(t)$ represents the square-root raised cosine pulse with roll-off factor ρ. Note that $g_T(t)$ is assumed to have unit energy in $[0, T_c]$ ($\int_0^{T_c} g_T^2(t)dt = 1$). For purposes of estimating the complex channel parameters $\{h_p(t), \tau_p(t)\}$ at the MS, a common pilot signal is broadcast by the BS to all mobile users [15, 25, 29]. The pilot signal can be provided either as a *code-multiplexed* or *time-multiplexed* channel. While the code-multiplexed pilot transmission is widely used in downlink transmission, the time-multiplexed pilot is need to implement a coherent uplink [20]. This thesis assumes that a code-multiplexed pilot signal is added to the spread signals of the individual users in the downlink.The pilot code $s_{pilot}(t)$,$0 < t < T_b$ is assumed to be known to all users, while the pilot symbols are an all-one sequence. Typically, the pilot is allocated higher power than the data signals corresponding to the individual

users. At the transmitter, the spread signals of all the users are added to generate a composite signal $u(t)$ represented by

$$u(t) = \sum_{i=0}^{N_b-1} \sum_{k=1}^{K} A_k b_{i,k} s_k(t - iT_b) + \sum_{i=0}^{N_b-1} A_{pilot} s_{pilot}(t - iT_b) \tag{2.2}$$

where N_b is the total number of transmitted information symbols, $b_{i,k}$ denotes the information symbol of the user k corresponding to the i^{th} signaling interval, $A_k = \sqrt{E_k}$ represents the transmit amplitude, and E_k is the energy per symbol for the k^{th} user. For purpose of simplicity, we assume that $A_k = A \, \forall k = 1 \ldots K$, therefore the pilot amplitude A_{pilot} is determined by the pilot-to-signal ratio (PSR) given by $PSR = 20 \log_{10}(\frac{A_{pilot}}{A})$ dB.

2.3 Received signal model

As described earlier in Section 2.1, the radio channel is modeled by a time-variant linear filter [25, 27] having the complex low-pass impulse response described by

$$h(t) = \sum_{p=1}^{P} h_p(t) \delta(t - \tau_p(t)) \tag{2.3}$$

where $h_p(t) = \alpha_p(t) e^{-j\theta(t)}$ denotes the time-varying complex channel coefficient of the p^{th} path, and $\tau_p(t)$ denotes the time-varying path delays constrained by the channel delay spread. We make two assumptions regarding the channel fading model. First, we assume that the channel coefficient amplitudes $\alpha_p(t)$ are Rayleigh distributed. Next, we assume that the fading amplitudes are constant over a symbol duration. Since we are considering the downlink transmission, the transmitted signals of all K users experience identical fading when receieved by any MS user. At the receiver, the received signal is down-converted to base-band after appropriate frequency and phase offset correction [17]. After down-conversion, the receiver signal at the MS denoted by $r(t)$ is represented by the convolution (denoted by $\otimes$) of the BS transmitted signal $u(t)$ and the channel filter impulse response

$h(t)$ given by,

$$\begin{aligned} r(t) &= u(t) \otimes h(t) + n(t) \\ &= \sum_{p=1}^{P} h_p(t) u(t - \tau_p) + n(t) \\ &= \sum_{p=1}^{P} h_p(t) \{ \sum_{i=0}^{N_b-1} \sum_{k=1}^{K} A_k b_{i,k} s_k(t - iT_b - \tau_p(t)) + \\ &\quad \sum_{i=0}^{N_b-1} A_{pilot} s_{pilot}(t - iT_b - \tau_p(t)) \} + n(t) \end{aligned} \tag{2.4}$$

where $u(t)$ is described by Equation 2.2, and $n(t)$ represents Additive White Gaussian Noise (AWGN).

2.3.1 Discrete-time sampling

The received continuous time signal is discretized by an Analog-to-Digital(A/D) converter by sampling $r(t)$ at the rate of $R = T_s^{-1} = \frac{NS}{T_b}$ samples per second, where T_s is the sampling time, N is the PN sequence length, S is the number of samples per chip, and T_b is the symbol duration. The equivalent discrete-time model representation of $r(t)$ is given by,

$$\begin{aligned} r(n) &= \sum_{p=1}^{P} \sum_{i=0}^{N_b-1} \sum_{k=1}^{K} h_{p,i}(n) A_k b_{k,i} s_k(n - iNS - n_p) + \\ &\quad \sum_{p=1}^{P} \sum_{i=0}^{N_b-1} h_{p,i}(n) A_{pilot} s_{pilot}(n - iNS - n_p) + w(n) \end{aligned} \tag{2.5}$$

where,

- $r(n)$ represents the discretized version of the continous-time signal $r(t)$.
- $h_{p,i}$ is the complex channel coefficient for the p^{th} path corresponding to the i^{th} symbol, and represents the discretized version of the continous-time channel variation $h_p(t)$.

- n_p is the sample discretized delay corresponding to the propagation delay τ_p of the p^{th} path.

- $s_k(n)$ is the signature sequence of the k^{th} MS user, representing the discrete version of the continous time user code spreading waveform $s_k(t)$.

- $w(n)$ is the discrete version of continous time AWGN represented by $\tilde{n}(t)$ with zero mean and two-sided spectral density $\frac{N_0}{2}$.

Signal-to-Noise Ratio at Receiver

Assuming that user 1 is the user of interest and that the fading remains constant over a symbol, the *average received energy per symbol* E_b with respect to user 1 can be written as

$$\begin{aligned} E_b &= \frac{1}{N_b}\sum_{p=1}^{P}\sum_{i=0}^{N_b-1}\sum_{n=iNS+n_p}^{(i+1)NS+n_p-1}|h_{p,i}(n)|^2 {A_1}^2 s_1^2(n-iNS-n_p) \\ &= \frac{1}{N_b}\sum_{p=1}^{P}\sum_{i=0}^{N_b-1}|h_{p,i}|^2\sum_{n=iNS+n_p}^{(i+1)NS+n_p-1}{A_1}^2 s_1^2(n-iNS-n_p) \\ &= \frac{1}{N_b}\sum_{p=1}^{P}\sum_{i=0}^{N_b-1}|h_{k,i}|^2 E_{b,tx} \\ &= E_{b,tx}\sum_{p=1}^{P}|\bar{h}_p|^2. \end{aligned} \tag{2.6}$$

where $E_{b,tx} = \sum_{n=0}^{NS-1} {A_1}^2 s_1^2(n)$ is the transmitted energy per symbol and $|\bar{h}_p|^2$ represents the variance of the channel coefficient h_p (assuming zero mean) corresponding to the p^{th} path. Note that we have assumed that the multi-path channel coefficients remain constant over a symbol interval ($h_{p,i}(n) = h_{p,i}$). The average received SNR is defined by

$$SNR = 10\log_{10}(\frac{E_b}{N_0}) \tag{2.7}$$

Vector-Matrix Notation

We can express Equation 2.5 in a more compact fashion through use of vector-matrix based notation [18] given by:

$$\mathbf{r}_i = \mathbf{S}\mathbf{H_i}\mathbf{A}\mathbf{b_i} + \mathbf{w}_i \tag{2.8}$$

where

- $\mathbf{r}_i$ is the received data vector corresponding to the i^{th} information symbol represented by

$$\mathbf{r}_i = \begin{bmatrix} r(iNST_s) \\ r((iNS+1)T_s) \\ \vdots \\ r([(i+2)NS-1]T_s) \end{bmatrix} \in \mathbb{C}^{2NS\times 1}$$

- $\mathbf{S}$ is the signature matrix for all K active users given by

$$\mathbf{S} = \begin{bmatrix} \mathbf{s}_{1,1}, & \ldots, & \mathbf{s}_{1,P}, & \ldots, & \mathbf{s}_{K,1}, & \ldots, & \mathbf{s}_{K,P} \end{bmatrix} \in \mathbb{R}^{2NS\times KP}$$

  Each of the columns $\mathbf{s}_{k,p}, 1 \leq k \leq K, 1 \leq p \leq P$ represents the appropriately delayed code of the k^{th} user corresponding to the p^{th} multi-path. Therefore,

$$\mathbf{s}_{k,p} = \begin{bmatrix} \mathbf{0}_{\lceil \frac{NS\tau_p}{T_b} \rceil \times 1} \\ \mathbf{s}_k \\ \mathbf{0}_{(SG-\lceil \frac{NS\tau_p}{T_b} \rceil)\times 1} \end{bmatrix} \in \mathbb{R}^{2NS\times 1}$$

  and

$$\mathbf{s}_k = \begin{bmatrix} s_k(T_s) \\ s_k(2T_s) \\ \vdots \\ s_k(NST_s) \end{bmatrix} \in \mathbb{R}^{NS\times 1}$$

where $s_k(t)$ represents the k^{th} user's continous-time spreading waveform given by the convolution of the user's spreading sequence $\{c_k(n)\}$and the transmitted chip-waveform $g_T(t)$.

- $\mathbf{H_i}$ denotes the complex channel impulse response coefficient matrix for the i^{th} information symbol given by

$$\mathbf{H_i} = \begin{bmatrix} \mathbf{h}_i & 0 & \dots & 0 \\ 0 & \mathbf{h}_i & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & \mathbf{h}_i \end{bmatrix} \in \mathbb{C}^{KP \times K}$$

where

$$\mathbf{h}_i = \begin{bmatrix} h_{i,1} \\ h_{i,2} \\ \vdots \\ h_{i,P} \end{bmatrix} \in \mathbb{C}^{P \times 1}$$

- $\mathbf{A}$ is the user amplitude matrix given by

$$\mathbf{A} = \begin{bmatrix} A_1 & 0 & \dots & 0 \\ 0 & A_2 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & A_K \end{bmatrix} \in \mathbb{R}^{K \times K}$$

- $\mathbf{b_i}$ is the symbol vector for all K users corresponding to the i^{th} transmission given by

$$\mathbf{b_i} = \begin{bmatrix} b_1 \\ b_2 \\ \vdots \\ b_K \end{bmatrix} \in \mathbb{R}^{K \times 1}$$

2.3.2 Rake receiver

First invented by Price and Green in 1958 [21], the RAKE receiver attempts to collect the signal energy from all the received signal paths that fall within the delay line and carry the same information [22]. For the DS-CDMA system, the RAKE receiver treats the interfering users as background noise, therefore it ignores the effect of the cross-correlations.

Assuming that user 1 is the user of interest, we defining the signature matrix,

$$\mathbf{S}_1 = \begin{bmatrix} \mathbf{s}_{1,1} & \mathbf{s}_{1,2} & \dots & \mathbf{s}_{1,p} \end{bmatrix} \in \mathbb{R}^{2NS \times P}$$

the RAKE receiver computes the decision statistic given by:

$$\begin{aligned} \hat{b}_{1,i} &= \text{sgn}(\mathbf{S}_1 \hat{\mathbf{h}}_i A_1)^H \mathbf{r}_i \\ &= \text{sgn}(\mathbf{S}_1 \hat{\mathbf{h}}_i A_1)^H (\mathbf{S}\mathbf{H}_i \mathbf{A} \mathbf{b}_i + \mathbf{w}_i) \end{aligned} \tag{2.9}$$

where $\hat{\mathbf{h}}_i \in \mathbb{C}^{P \times 1}$ is the complex channel coefficient estimate obtained from the output of a channel estimator. To estimate the complex channel coefficient for performing phase offset correction, a channel estimator is required. In this thesis, we assume a L tap moving average filter for channel estimation while demodulating the i^{th} information symbol. The pilot symbol sequence is assumed to be known at the receiver and is used for the purpose of channel estimation. For the pilot sequence, we can define

$$\mathbf{S}_{pilot} = \begin{bmatrix} \mathbf{s}_{pilot,1} & \mathbf{s}_{pilot,2} & \dots & \mathbf{s}_{pilot,p} \end{bmatrix} \in \mathbb{R}^{2NS \times P}$$

as the pilot code signature matrix. Then, the channel estimate $\hat{\mathbf{h}}_i$ is given by the expression

$$\hat{\mathbf{h}}_i = \sum_{i=n-L+1}^{n} b_{1,i}^* \mathbf{S}_{pilot}^H \mathbf{r}_i \tag{2.10}$$

where L is the length of the averaging filter.

In the next chapter, we describe the design methodology followed during the implementation of the DS-CDMA downlink RAKE receiver.

Chapter 3

Design Methodology for the RAKE receiver

This chapter examines the design methodology involved in the FPGA based synthesis of the DS-CDMA RAKE receiver for a mobile handset. Beginning with a description of the algorithm design phase, the chapter proceeds to describe the various steps involved while proceeding from a conceptual description to an actual prototype of the DS-CDMA RAKE receiver.

3.1 Overview

Figure 3.1 shows the flow of a System-on-chip (SoC) design cycle [14]. The design cycle follows a top-down approach starting from the algorithm design phase culminating in the fabrication of the completed SoC. The initial phase starts with the formulation of the algorithm to cater to the design specifications. By performing extensive floating-point level simulations, the system designer tries to refine the algorithm parameters, in order to achieve improved algorithm performance. Depending on the type of application under consideration, the algorithm is targeted towards either a floating-point or fixed-point arithmetic based architecture. Assuming a fixed-point approach, the design cycle then proceeds with the determination of the dynamic range and precision requirements of the algorithm parameters. Typically, the aforementioned operations entail going up the hierarchy and repeating the cycle to achieve a better performance. For example, if the fixed-point version of an algorithm under-performs with respect to the floating point version on account of excessive

scaling, then the application parameters may need to be modified for obtaining better fixed-point behavior. After fixed-point analysis, a target architecture is devised for a hardware

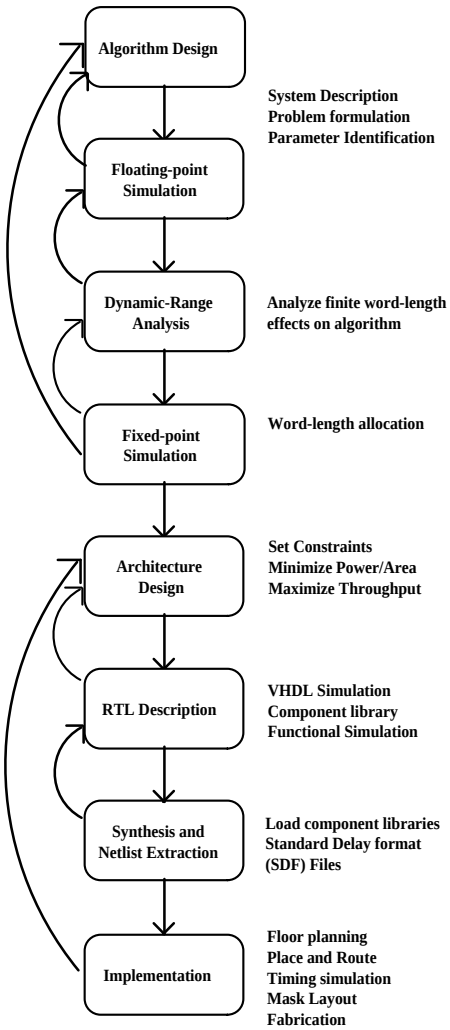

Figure 3.1 : A Typical VLSI design flow

implementation that is optimized with respect to a specific criterion. For instance, the architectural design of a mobile terminal receiver would be targeted towards *minimizing the dynamic power-dissipation* [8, 9]. On the contrary, the design of a base-station architecture would focus on *maximizing the throughput* and meeting real-time target data-rates for

all mobile users [24]. Architectural techniques such as parallelism and pipelining can be effectively employed to achieve either of the above constraints [9]. The RTL description of the architecture is followed by functional simulation to verify correctness of boolean logic. Logic synthesis is carried out where the RTL description is mapped into a synthesizable net-list. The final phase involves the actual VLSI implementation comprising steps such as floor-planning, placement and routing, performing gate-level timing simulations, mask-layout and fabrication.

3.2 Rake receiver: Design methodology

3.2.1 Algorithm design phase

The first step namely the Algorithm design phase involves the design of the DS-CDMA RAKE receiver within the specifications (refer Table 3.1) of the system. The specifications were chosen in order to:

- Realistically model phenomena such as received signal amplitude degradation and phase distortion arising out of characteristics of the wireless channel such as multi-path fading, presence of noise etc.
- Attempt to closely follow existing industry standards such as the Interim Standard 95 (IS-95), and as well as future 3G-based standards such as UMTS [12], CDMA2000 [13] etc.

For characterizing the performance of the receiver, floating point simulations were carried out in the MATLAB environment with additional back-end C routines for providing speed-up in simulation.

PARAMETER	**SPECIFICATION**
Spreading Waveform	Extended PN Gold sequences
Processing Gain(N)	32
Modulation Type	BPSK
Spreading Waveform	Square root-raised cosine
Pilot-to-signal ratio (PSR)	3 dB
Roll-off factor (ρ)	0.22
Data-rate	$384,000$ symbols/s
Carrier frequency	2 Ghz
Channel Delay Spread	2.6μs(1 symbol)
Number of resolvable paths	3
Maximum mobile velocity	70 mph
Channel Fading type	Correlated Rayleigh
Receiver chip-sampling rate(S)	2 samples/chip
Sampling-rate at receiver A/D	24.576 MSamples/s
Channel Estimator at receiver	16 tap MA filter

Table 3.1 : Design specifications for the RAKE receiver

3.2.2 Quantization Analysis

Pros and cons of a fixed-point approach

The advantages of a fixed point approach are the reduced design costs in terms of silicon area and power consumption. Fixed-point designs typically have higher speeds and throughput compared to floating point designs. The choice of fixed-point is heavily influenced by the application characteristics such as the dynamic range, signal-to-noise (SNR) and type of arithmetic operations involved. Dynamic range refers to the ratio between the largest and smallest representable numbers in the data format. For example, a 32 bit fixed-point Digital Signal Processor (DSP) has a dynamic range of approximately 187 dB while a 32 bit floating-point DSP has a dynamic range of 1535 dB. In terms of application requirements, constructed signals such as telecommunication applications and high-fidelity audio applications have dynamic ranges of 50 dB and 90 dB respectively and perform very well in fixed-point based architectures. On the other hand, real-world signals such as radar, sonar and radio signals have larger dynamic range (more difficult to scale) and hence require floating-point based architectures to accommodate the dynamic range of the algorithm [6]. Since the fixed-point approach requires scaling at the input of the system by use of Automatic Gain Control (AGC) based techniques, the noise-floor of the application also plays an important role in determining the efficiency of the algorithm in fixed-point. Fixed-point approaches perform best for systems having a large input SNR, in order that input scaling does not significantly affect the ability of the algorithm to separate the signal from background noise. Lastly, the operations performed in the application can significantly impact the ease of implementation of fixed-point design. Applications in mobile telecommunications such as multi-user detection (at base-stations), adaptive beamforming usually require repetitive matrix inversions which may be extremely difficult to implement in fixed-point

arithmetic, owing to the increased sensitivity of these operations on quantization effects. All the DS-CDMA architectures presented in this thesis are based on a fixed-point implementation. The rationale behind this is that

- Portable devices such as laptops, PDA's, cell-phones have limited battery life, and therefore inherently have stringent low-power requirements. Such devices cannot facilitate the use of dedicated floating point units on account on their slower operation, greater power consumption and area requirements.

- Based on rigorous simulations (discussed in Chapter 6), we show that the fixed-point based RAKE algorithm performs within 1 dB of the corresponding floating point implementation. This shows the robustness and numerical stability of the detector to finite word-length effects.

Selection of fixed-point word-lengths

The fixed-point phase begins with determining the dynamic range and precision requirements of the individual variables in the algorithm. Careful selection of fixed-point precision is necessary in order to avoid potential overflows and underflows during intermediate computations. The choice of word-length is primarily influenced by two factors namely:

- Target performance of the fixed-point based algorithm in comparison with a floating point implementation: For example, the design of a fixed-point based wireless communications receiver would be influenced by the target bit-error rate requirement of the implementation, in order to determine the optimal word-lengths for individual variables. The precision of the individual variables can be continually reduced as long as the algorithm performance is not significantly deteriorated.

- Nature of the targeted implementation: Depending on the type of application, the algorithm may either be implemented using a direct-mapped approach such as an Application Specific Integrated Circuit (ASIC), or a processor like approach akin to a fixed-point DSP. An design targeted for an ASIC-based implementation would allow for customized word-lengths tailored to suit the word-length requirements of individual variables. A DSP-based approach, on the other hand, would require a uniform precision for all variables, on account of the uniform data-path width on a DSP.

A quantization analysis tool developed at the University of Texas, Dallas [19] was used for determining the dynamic range and precision requirements of the detector. The tool collects the dynamic range statistics of the different detector variables under test, from the floating point C version of the RAKE algorithm. Using an interactive MATLAB program, the dynamic range of the various variables are determined by means of a histogram based GUI, and used to fix the precision requirements of the individual variables. This thesis assumes that all the fixed-point variables are quantized with a uniform width and only differ in their integer bit requirements.

Using the specifications shown in Table 3.1, the dynamic range statistics of the RAKE receiver variables were collected. Table 3.2 shows the fixed-point integer requirements of the individual RAKE receiver variables after quantization analysis. The corresponding fractional bit-width requirements were determined from the difference of the overall precision and the number of integer bits. From the obtained fixed-point formats in Section 3.2.2, extensive simulations were carried out using MATLAB/C with C++ classes in SystemC [3] providing the fixed-point arithmetic support (explained in greater detail in Chapter 6).

Detector Variable	Description	Integer bits
$\mathbf{r}_i \in \mathbb{C}^{2NS\times 1}$	Complex receiver input data	1
$\mathbf{S}_1 \in \mathbb{R}^{2NS\times P}$	User signature matrix	1
$\mathbf{S}_{pilot} \in \mathbb{R}^{2NS\times P}$	Pilot signature matrix	1
$\mathbf{S}_1^H \mathbf{r}_i \in \mathbb{C}^{P\times 1}$	Soft Rake Correlator Output	3
$\mathbf{S}_{pilot}^H \mathbf{r}_i \in \mathbb{C}^{P\times 1}$	Soft Pilot Correlator Output	3
$\sum_{k=i-L+1}^{i} b_{1,k}^* \mathbf{S}_{pilot}^H \mathbf{r}_k \in \mathbb{C}^{P\times 1}$	Moving Average Accumulator	5
$\hat{\mathbf{h}}_i = E[b_{1,i}^* \mathbf{S}_{pilot}^H \mathbf{r}_i] \in \mathbb{C}^{P\times 1}$	Channel coefficient Estimate	3
$(\mathbf{S}_1 \hat{\mathbf{h}}_i A_1)^H \mathbf{r}_i \in \mathbb{C}^{1\times 1}$	Maximal Ratio Combiner output	6

Table 3.2 : Fixed-point precision requirements for the RAKE receiver

3.2.3 Implementation aspects

For purposes of implementing the DS-CDMA RAKE architecture (a detailed description of the architecture is provided in Chapter 4, a Field Programmable Gate Array (FPGA) based approach was chosen. The main motivation behind the use of the FPGA is the ability to rapidly prototype applications on hardware without incurring the cost and delay associated with building custom CMOS VLSI architectures.

Overview of a FPGA

A FPGA is a type of programmable device, that has evolved from earlier programmable devices such as the PROM (Programmable Read-only memory), the PLD (Programmable logic device), and the MPGA (Mask Programmable Gate Array).There are four main categories of FPGAs currently available commercially: symmetrical array, row-based, hierarchical PLD, and sea-of-gates. In all of these FPGAs the interconnections and how they are

programmed vary. Currently there are four technologies in use. They are: static RAM cells, anti-fuse, EPROM transistors, and EEPROM transistors. Depending upon the application, one FPGA technology may have features desirable for that application [4].

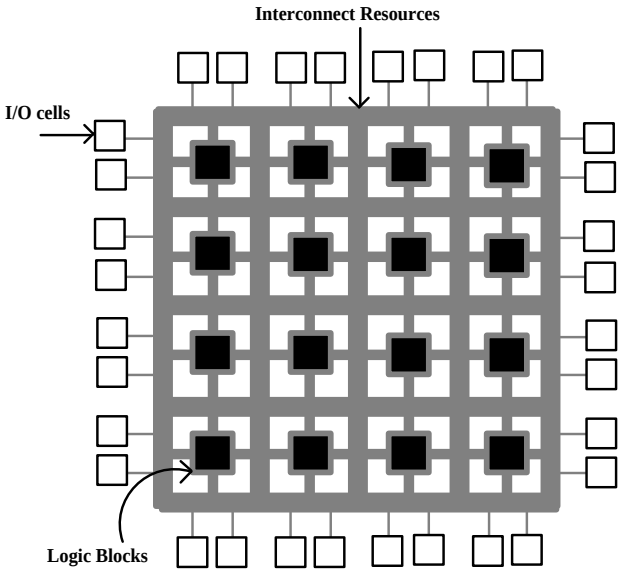

Figure 3.2 : Conceptual diagram of a FPGA

A FPGA (refer Figure 3.2) has three major configurable elements: configurable logic blocks (CLBs), input/output blocks, and interconnects. The CLBs provide the functional elements for constructing user's logic. The IOBs provide the interface between the package pins and CLBs. The programmable interconnect resources provide routing paths to connect the inputs and outputs of the CLBs and IOBs onto the appropriate networks. Customized configuration is established by programming internal static memory cells that determine the logic functions and internal connections implemented in the FPGA.

In this work, we have employed a Xilinx Virtex-II 1.5 V FPGA that employs a symmetrical array architecture with the static RAM based programmable interconnections. This FPGA has been fabricated with a 0.15μm CMOS 8 layer metal process. Its architecture

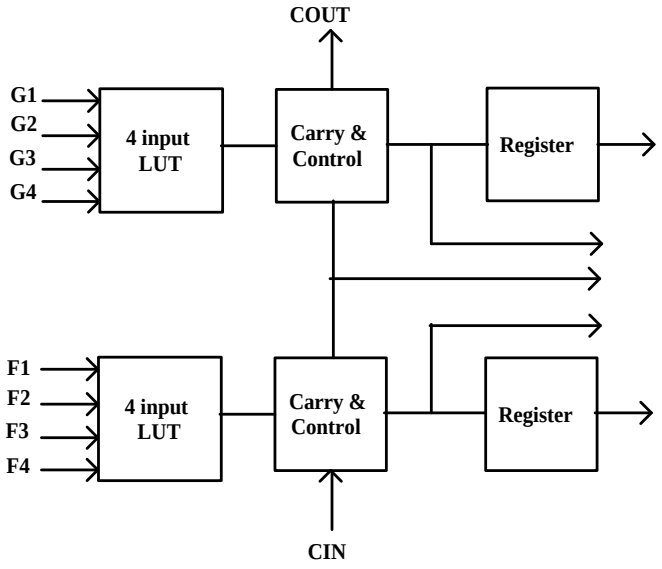

Figure 3.3 : A CLB Slice in the Virtex-II FPGA

has been optimized for high speed with low power consumption. The Virtex-II FPGA's are capable of supporting high density designs with areas up to 10 million gates. As typical designs employ multiple clocking domains, all Virtex-II devices have 16 global clock buffers and support 16 global clock domains, with a maximum internal clocking speed of 420 MHz [5]. Additional features include DCM's (Digital Clock Manager) for generating of de-skewed clocks, as well as fine-grained phase shifting for high resolution phase adjustments in increments of $\frac{1}{256}$ of the clock period.

Figure 3.3 shows a CLB slice inside the FPGA. The basic building block of a CLB is the logic cell. Each Logic cell includes a 4-input function generator, carry logic and a register (storage element). The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each CLB contains four LCs organized in two similar slices. Each CLB has fast interconnect and connects to a switch matrix to access general routing resources.

Design Modeling, Logic Synthesis and Power Estimation

The reference and power-optimized versions of the DS-CDMA RAKE receiver were implemented in the Xilinx ISE design environment. The Register-Transfer Level (RTL) description was performed with VHDL [10]. Logic Synthesis and netlist extraction was performed using Synplify Pro. Finally, the power estimation was carried out using the XPower power analysis tool [1] from Xilinx.

In this chapter, we have described the VLSI design methodology followed during the design of the mobile RAKE receiver. The next chapter proceeds to give a detailed description of the mobile RAKE receiver architecture and highlights the functionality of the individual blocks.

Chapter 4

The DS-CDMA RAKE receiver architecture

This chapter discusses the reference architecture for the RAKE receiver employed in the DS-CDMA downlink. We elaborate the architecture following a top-down approach, starting from a “black-box” level abstraction, and consequently focus on individual sub-blocks as the chapter proceeds. Towards the end, we hint towards potential optimizations that can reduce the dynamic power consumption, thus providing the motivation for subsequent chapters.

4.1 System Description

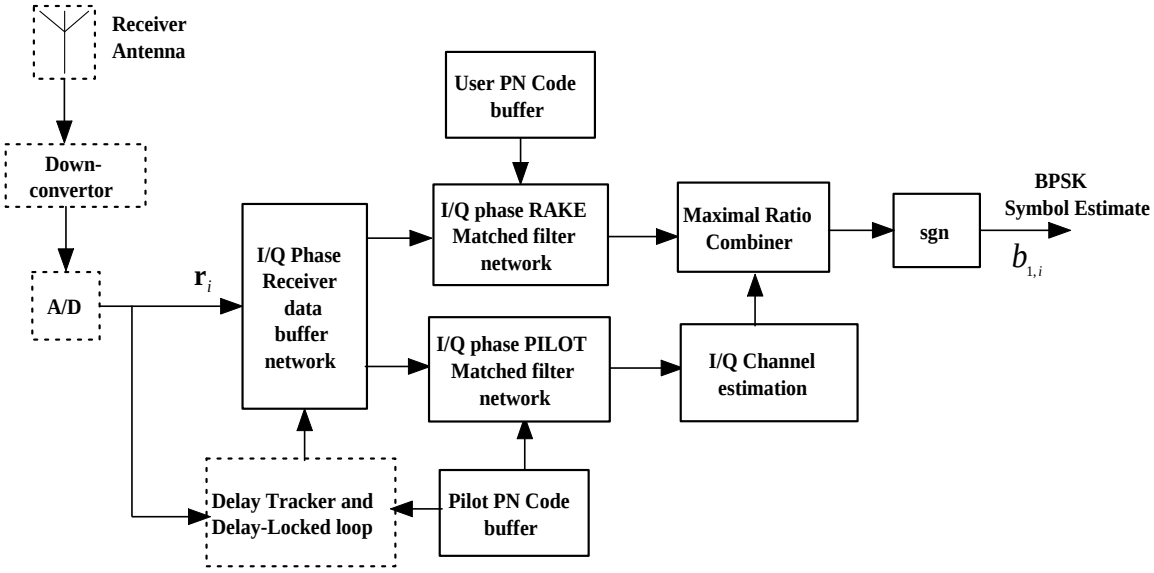

Figure 4.1 : Front-end description of a wireless communication DS-CDMA receiver

Figure 4.1 shows the high-level description of the front-end in a wireless communication receiver. The architectures implemented in this thesis are represented by the solid line blocks(corresponding to the RAKE receiver), while the dashed-line blocks are assumed to feed in the sampled wide-band signal and the estimated delays into the receiver. As mentioned earlier in Chapter 2, the received continuous time signal $r(t)$ is discretized by sampling at the rate $R = T_s^{-1} = \frac{NS}{T_b}$ where T_s is the sampling time, N is the PN sequence length, S is the number of samples per chip, and T_b is the symbol duration. The user and pilot code sequences are allocated from extended PN Gold sequences of length $N = 32$ at an oversampling rate of $S = 2$ samples/chip (refer Table 3.1 in Chapter 3 for the specifications of the design). The sampled complex wide-band receiver data is input to the RAKE receiver for performing symbol-level demodulation, and the delay-tracker block for initial timing acquisition followed by fine synchronization with a delay-locked loop. For the i^{th} symbol interval, complex receiver data $\mathbf{r}_i$ is input to the RAKE receiver in a chip-serial fashion. The RAKE receiver unit comprises the following principal blocks:

- Front end circular buffer for storing complex receiver data to be used for performing correlation during the channel estimation and detection operations.

- User/Pilot PN code circular buffer of size $NS = 64$ for storing the user and pilot signature sequences for correlation with the complex receiver data. For the reference architecture, we assume that both the RAKE and the PILOT correlators employ a uniform sampling rate of $S = 2$ samples per chip for processing the receiver data.

- In-phase and Quadrature-phase RAKE/PILOT matched-filtering block for performing the correlation with the transmitted waveform and output soft symbol-level correlations over all paths.

- Channel estimator block for estimating the instantaneous complex channel coeffi-

cients over all paths.

- Maximal Ratio Combiner block for weighting the complex soft correlation output from the RAKE correlator block with the estimated complex channel coefficient.

The following sections describe the individual blocks and their respective functionality.

4.2 Front end circular buffer

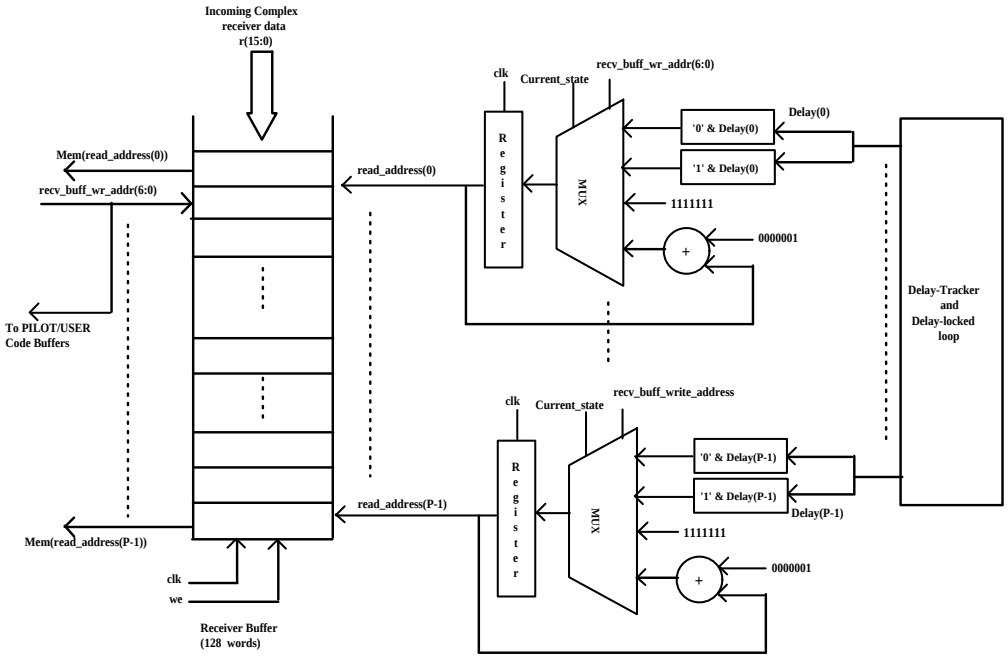

Figure 4.2 : Buffer for storing complex receiver data

The front end circular buffer serves the purpose of buffering up sufficient complex receiver data in order to ensure that the RAKE/PILOT correlator units do not stall when the channel delays change abruptly. The required buffer size is a function of the multi-path propagation delay of the channel and the symbol-rate employed in the system. For a delay spread of D chips and processing gain of $N = 32$ chips, the minimum buffer size

is given by $B = NS * \lceil \frac{D}{N} + 1 \rceil$ words. The corresponding *Read/Write* address-line width equals $\lceil \log_2 B \rceil$ bits. For the reminder of this thesis, it is assumed that the maximum delay spread equals one symbol, therefore the buffer size equals $B = 2NS = 128$ words and the corresponding address-line width equals $\lceil \log_2 128 \rceil = 7$ bits. This assumption is quite reasonable since typical observed channel delay-spreads are less than a symbol at data rates up to 384 kbps (refer Table 2.1 in Chapter 2). The design of the buffer becomes more complicated if the allowable delay spread is greater than a symbol, and is outside the scope of this thesis. Figure 4.2 shows the structure of the receiver circular buffer for $N = 32$, $S = 2$. The delay-spread is assumed to be a symbol duration ($NS = 64$ samples). The buffer employs the following modes of operation:

- **Initialization mode**: This mode is employed only at the beginning of operation of the RAKE receiver in order to initialize the contents of the buffer. For the first $NS = 64$ cycles, the buffer is written into, till there is a symbol-duration worth of receiver data stored in the buffer. During this period, all the read-addresses are set to a value of 128 to ensure that there is no memory access conflict generated by the read and write addresses. The receiver data is written into the $recv\_buff\_wr\_addr$ specified from 0 to $NS - 1 = 63$. When $recv\_buff\_wr\_addr = NS = 64$, the mode changes to the steady-state mode described below.

- **Steady state mode**: At the end of the Initialization mode, there are $NS = 64$ words of receiver data (or 1 symbol worth of information) stored in the buffer. Conditioned on the current value of $recv\_buff\_wr\_addr$, the read-port address $read\_address(i), i = 0 \ldots P - 1$ is either initialized with the computed path delays $Delay(i)$ (from the delay-tracker and delay-locked loop unit), or incremented by one. The read-port

addresses are specified by,

$$Read\_Address(i) = \begin{cases} Delay(i) & \text{if } recv\_buff\_wr\_addr = 64 \\ Delay(i) + 64 & \text{if } recv\_buff\_wr\_addr = 0 \\ Read\_Address(i) + 1 & \text{otherwise} \end{cases}$$

The values of the write-address namely $recv\_buff\_wr\_addr = NS + 1 = 65$ and $recv\_buff\_wr\_addr = 1$ signify the beginning of a new correlation operation for detecting a new symbol, after the appropriate multi-path delays have been loaded in the previous cycle. As the read-addresses get incremented, successive complex receiver data values get read from the buffer and are input to the RAKE/PILOT correlator units where the correlation of the receiver data with the user/pilot codes is carried out.

Implementation issues

For a P finger RAKE receiver, the above description assumes a receiver buffer with P read-ports each for the real and imaginary parts of the complex receiver data. In a practical implementation however, truly multi-ported buffers are infeasible owing to the high output load capacitance which would dramatically increase the memory access time, and hence the operating frequency of the design. One possibility is to use a parallel register file based data structure [16] to store the 128 words of receiver data. The drawback with this approach is the excessive loading of the data bus, as well as the huge multiplexer banks required to access the appropriately delayed multi-path data corresponding to each RAKE/PILOT correlator finger. Another alternative is to use a serial shift register delay line implementation. For a n bit data-path, there are $\frac{n}{2}$ logic transitions (for real and imaginary data storage registers) potentially occurring at every node per clock cycle, due to shifting of data in the shift register unit [16, 26]. For the shift register storage size of $2NS = 128$ words of n

bit receiver data, this would amount to an average of $NSn = 64n$ logic transitions per clock cycle which is clearly power-inefficient. Consequently, a much simpler approach was adopted by instantiating P separate SRAM based dual-ported receiver data buffers, to store the real and imaginary components of the input sampled receiver data. This ensures a smaller output load capacitance at the data-bus compared to the register-file based approach. Moreover, the use of the pointer-based approach implies that the switching activity in the data-bus is reduced from $NSn = 64n$ logic transitions to just $Pn/2 = 1.5n$ logic transitions per clock cycle on an average. The tradeoff with this approach is that the same receiver data is stored in P separate buffers. *

4.3 User/Pilot code circular buffer

The User/Pilot code circular buffers (Figure 4.3) store the length $NS = 64$ PN sequences of the user ($\mathbf{s}_1 \in \mathbb{R}^{64\times1}$) and pilot codes ($\mathbf{s}_{pilot} \in \mathbb{R}^{64\times1}$). In this thesis, we assume that the code coefficients are pre-determined at start-up and stored in the buffer. Since the symbol despreading operation begins when $recv\_buff\_wr\_addr = 1$ or $recv\_buff\_wr\_addr = 65$, the read-address pointer $code\_read\_addr$ (6 bits wide) for the buffer is directly determined by the current write address $recv\_buff\_wr\_addr$ of the front end circular buffer described in Section 4.2, by the relation $code\_read\_addr = recv\_buff\_wr\_addr \mod 64$. In other words, while $recv\_buff\_wr\_addr$ counts from 0 to $2NS-1 = 127$, $code\_rd\_addr$ counts from 0 to $NS - 1 = 63$.

---

*In future, we aim to explore an alternative scheme by which the bank of P memories could be replaced by a single dual-ported memory which would feed appropriately delayed receiver data to the despreading units. However, the drawback with this approach is that the despreading operations in the RAKE and PILOT correlators would not longer begin simultaneously. The beginning and end of the correlation in any finger would be dictated by the time arrival of the corresponding path.

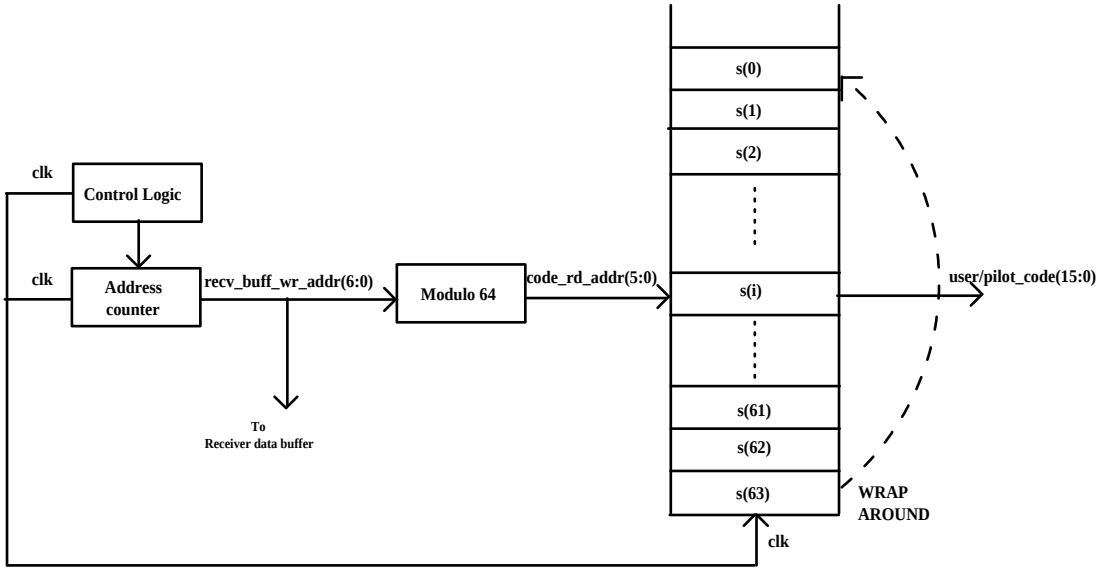

Figure 4.3 : Circular buffer for storing the user/pilot code coefficients

4.4 PILOT and RAKE Matched-filter blocks

At a high level, the PILOT and RAKE correlator blocks (see Figure 4.4) take in the sampled wide-band signal, perform matched-filtering, and output a narrow-band signal at the symbol rate. The narrow band output and channel estimates are fed to the Maximal Ratio combiner which performs coherent demodulation.

Figure 4.5 illustrates the architecture of the PILOT/RAKE finger correlator network for computing the complex inner products, $pilot\_soft\_out(i) = \mathbf{S}_{pilot}^{H}\mathbf{r}_i$ and $rake\_soft\_out(i) = \mathbf{S}_{1}^{H}\mathbf{r}_i$ where $i, 0 \leq i \leq P-1$ corresponds to the i^{th} finger and $\mathbf{r}_i$ refers to the delayed multipath data coming from the receiver circular buffer.

4.4.1 Correlator: Pipelined Multiply Accumulate (MAC) unit

The i^{th} PILOT/RAKE correlator employs a Multiply-accumulate unit for performing the inner product computation. Figure 4.6 shows the structure of the pipelined MAC unit. The

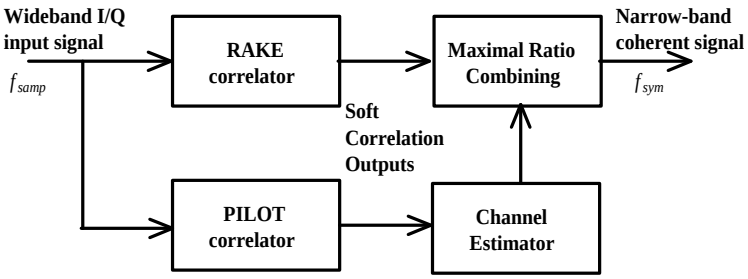

Figure 4.4 : High level block diagram of the PILOT/RAKE correlators

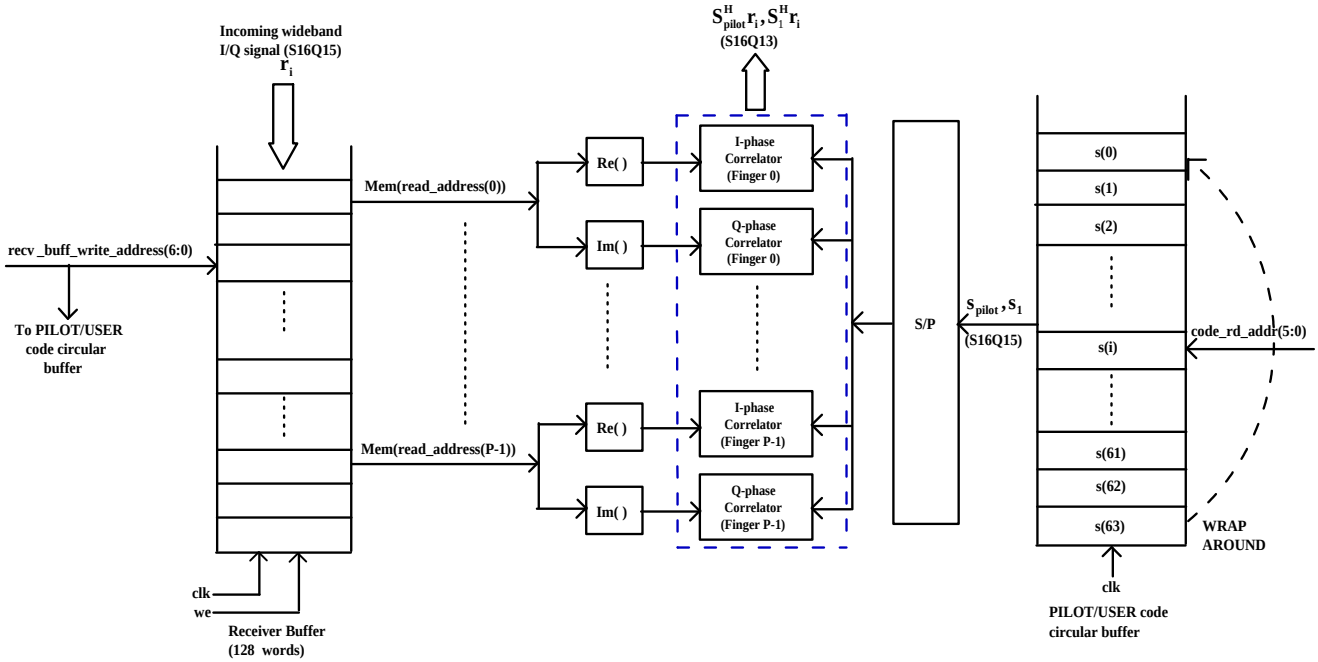

Figure 4.5 : Structure of the PILOT/RAKE finger network

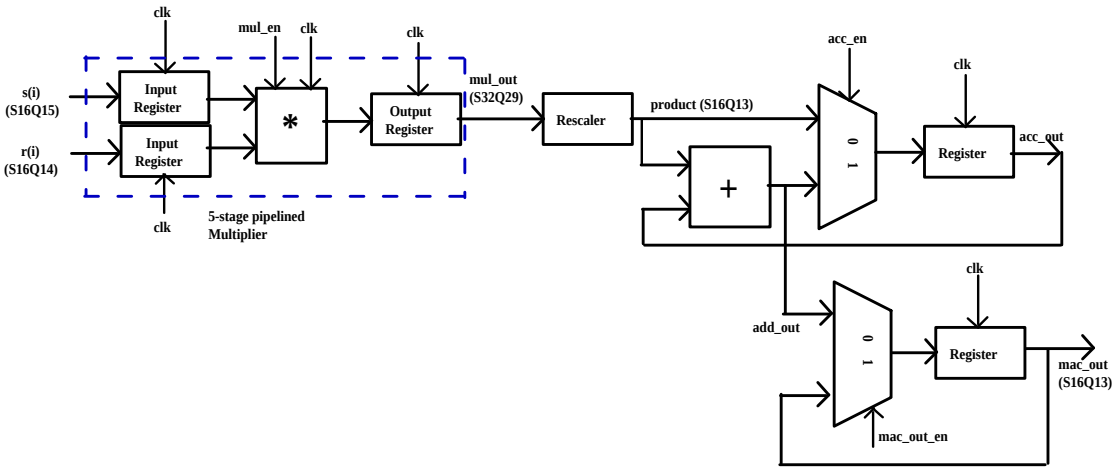

Figure 4.6 : Structure of the MAC unit

MAC unit takes the N-bit precision inputs $r(i)$,$s(i)$ where $0 \leq i \leq M-1$ and computes the sum,

$$S = \sum_{i=0}^{63} r(i)s(i) \tag{4.1}$$

In Figure 4.6, it is assumed that N=16, operand $s(i)$ has the fixed-point format $S16Q15$, operand $r(i)$ has the fixed-point format $S16Q14$, and the MAC output mac_out has the format $S16Q13$. Although the design of a MAC unit is intuitive and conceptually simple, the efficient operation of the unit depends on factors such as,

1. Absence of any pipeline stalls during the starting of any MAC operation. After the completion of the j^{th} MAC operation, there should ideally be no stalls for reinitializing the accumulator contents to begin the computation of the $(j+1)^{th}$ MAC operation.

2. Ability to operate the MAC unit at a high clocking frequency irrespective of the precision requirements of the input operands. Typically, the unpipelined multiplier acts as the critical path for determining the clocking rate of the MAC unit. By internally

pipelining the multiplier, this bottleneck can be alleviated to a great extent.

The control of the MAC unit operation is performed by three control signals namely *mul_en*, *acc_en*, and *mac_out_en*. The multiplier has a 5-stage pipeline (including the input and output registers shown in the Figure 4.6). To begin the j^{th} MAC operation, the multiplier is enabled by setting *mul_en*=1 after the arrival of valid inputs $r(0)$, $s(0)$ at the rising edge of clock cycle 0. The control signal *mul_en* is held high for the entire duration of the MAC operation. The 1^{st} product $mul\_out = r(0)s(0)$ appears at the output register of the multiplier at the rising edge of clock cycle 5. Since the precision at the output of the multiplier is double the input operand precision, the multiplier output is rescaled to suit the fixed-point format of the MAC output *mac_out*. As long as *acc_en*=0, the node *acc_out* equals *product*. To start the accumulation operation, *acc_en* is enabled at the rising edge of clock cycle 6, and held high as long as the current MAC operation is going on. The M^{th} product appears at the rising edge of clock cycle $M + 4$. The control signal *mac_out_en* is asserted at the rising edge of the same clock cycle and the computed MAC output $S = \sum_{i=0}^{M-1} r(i)s(i)$ appears in the rising edge of cycle $M + 5$. Simultaneously, *acc_en* is held low and reasserted at the rising edge of clock cycle $M + 6$ to start the accumulation for the $(j + 1)^{th}$ MAC operation.

4.5 Moving averager filter based Channel Estimation

The channel estimator block uses a simple moving averager filter to estimate the complex multi-path channel co-efficients. For the i^{th} symbol demodulation, the estimated channel coefficient $\hat{\mathbf{h}}_i \in \mathbb{C}^{P\times 1}$ is computed by,

$$\hat{\mathbf{h}}_i = \frac{1}{L} \sum_{k=n-L+1}^{n} b^*_{pilot,k} \mathbf{S}^H_{pilot} \mathbf{r}_k \tag{4.2}$$

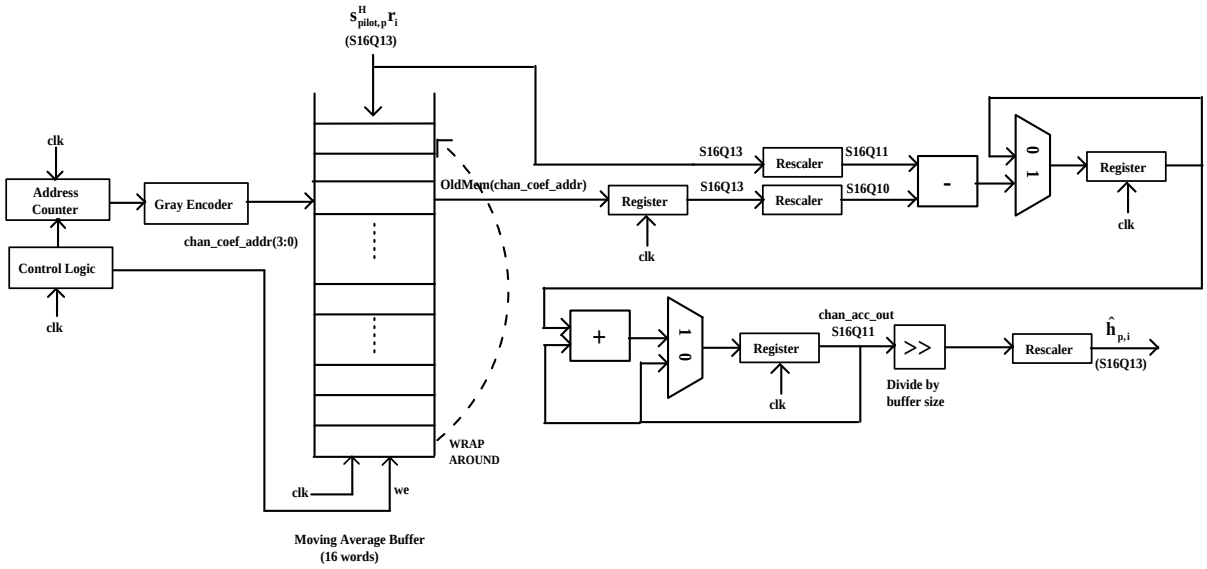

Figure 4.7 : Moving Average based channel estimation

The expression for $\hat{\mathbf{h}}_i$ in Equation 4.2 assumes that the channel is slow fading over the block of L symbols. For a slow fading channel, choosing a large L helps in mitigating background interference. Since the filtering operation (see Figure 4.7) computes the channel estimates based on the results of the previous L pilot correlations, a L word circular buffer based implementation is employed. As mentioned earlier in Section 4.2, a circular buffer-based implementation consumes lesser power than a delay line based shift register structure, due to the smaller number of logic transitions on the data bus. In the practical implementation, the pilot sequence is assumed to be an all ones sequence, therefore, the computation of $\hat{\mathbf{h}}_i$ is simplified as shown,

$$\hat{\mathbf{h}}_i = \hat{\mathbf{h}}_{i-1} + \{\mathbf{S}_{pilot}^H(\mathbf{r}_i - \mathbf{r}_{i-L})\} \gg \lceil log_2 L \rceil \tag{4.3}$$

Corresponding to symbol i, the despread pilot correlation output $\mathbf{S}_{pilot}^H \mathbf{r}_i$ is written into the circular buffer address $i \mod L$ where it replaces the oldest pilot correlation output $\mathbf{S}_{pilot}^H \mathbf{r}_{i-L}$. The difference between these two values is used to compute the i^{th} channel

estimate as indicated in Equation 4.3. A “read before write” type of circular buffer is chosen for implementation, in order that the oldest pilot correlation value is read out before being overwritten by the new pilot correlation output. For performing the scaling, L is chosen to be a power of 2, in order to replace the division operation by right shifting by L bits (as a shifting operation is implemented with a barrel shifter avoiding specialized circuitry for performing division).

4.6 Maximal Ratio Combining

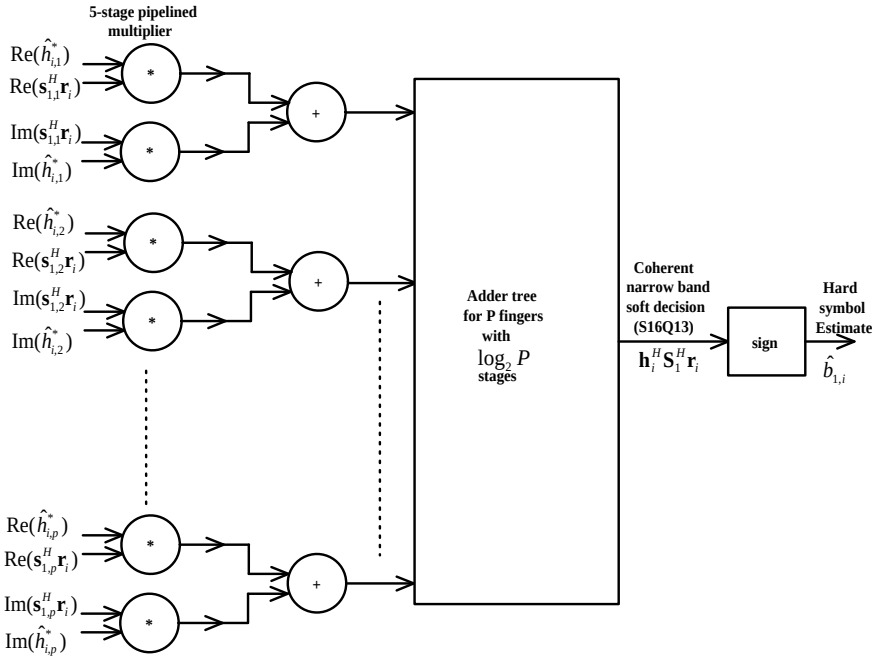

Figure 4.8 : Maximal Ratio Combiner unit

The Maximal Ratio Combiner (MRC) weights the narrow band despread outputs of the RAKE finger network, by the corresponding complex conjugated channel coefficient estimates. This is equivalent to combining the multi-path symbol estimates according to the

relative path strengths. Figure 4.8 shows the implementation of the MRC unit. The 5 stage pipelined multipliers implement the phase rotation operation $\hat{\mathbf{h}}_i^H \mathbf{S}_1^H \mathbf{r}_i$. The $\lceil \log_2 P \rceil$ stage deep adder tree network combines the phase rotated outputs and produces a single soft symbol estimate. Since this thesis assumes that BPSK symbol modulation is employed, only the real component of the MRC operation is required. Finally, the hard symbol estimate $b_{1,i}$ corresponding to the i^{th} transmitted symbol of user 1 is computed by taking the sign of the MRC output as shown in Equation 4.4.

$$b_{1,i} = \text{sgn}(\text{Re}(\hat{\mathbf{h}}_i^H \mathbf{S}_1^H \mathbf{r}_i)) \tag{4.4}$$

In this chapter, we have discussed the practical implementation aspects of the various blocks constituting the DS-CDMA RAKE receiver architecture. The next chapter describes the various low-power design methodologies that were pursued in order to reduce the power requirements of the above architecture.

Chapter 5

Power-reduction methodologies for the DS-CDMA RAKE receiver

This chapter elaborates on the different techniques employed to reduce the dynamic power dissipation in the DS-CDMA RAKE architecture discussed in the previous chapter. The techniques were implemented at different stages of the design cycle (outlined in Figure 3.1 in Chapter 3). Starting with a brief overview of power-reduction techniques in VLSI circuits, the chapter proceeds to describe the methodologies specific to the design of the DS-CDMA RAKE demodulator. At the algorithmic level, we describe a simple power-optimization namely the reduction in the arithmetic complexity of the despreading operation in the RAKE receiver, and its impact on the resulting architecture. At the architectural level, we investigate techniques such as reduced precision and activity rate reduction through clock-gating techniques for additional power savings.

5.1 Overview

Dynamic power dissipation is usually the dominant source of power dissipation in CMOS VLSI circuits. The dynamic power consumption P_{dyn} at any node in a CMOS-based design is a function of the node capacitance C, the switching activity α of the node [defined as the average number of node transitions per clock cycle], the clocking frequency f_{clock}, and the supply-voltage V_{cc} employed in the design, given by Equation 5.1

$$P_{dyn} = \frac{1}{2}\alpha C {V_{cc}}^2 f_{clock} \tag{5.1}$$

Operation	Multiplications	Additions
$\mathbf{S}_1^H \mathbf{r}_i \in \mathbb{C}^{P\times 1}$	$4NP/2NP$	$2P(2N-1)/2P(N-1)$
$\mathbf{S}_{pilot}^H \mathbf{r}_i \in \mathbb{C}^{P\times 1}$	$4NP$	$2P(2N-1)$
$\hat{\mathbf{h}}_i = \frac{1}{L}\sum_{k=i-L+1}^{i} {b_k}^* \mathbf{S}_{pilot}^H \mathbf{r}_k \in \mathbb{C}^{P\times 1}$	-	$2P(L-1)$
$\mathrm{Re}(\hat{\mathbf{h}}_i^H \mathbf{S}_1^H \mathbf{r}_i) \in \mathbb{R}^{1\times 1}$	$2P$	$2P-1$
RAKE receiver (2 samples/chip)	$(16NP + 2LP - 2P - 1)$ flops	
RAKE receiver (1 sample/chip)	$(12NP + 2LP - 2P - 1)$ flops	

Table 5.1 : Arithmetic complexity per symbol detection in the Reference and Reduced Complexity DS-CDMA RAKE receivers employing BPSK signaling

Since P_{dyn} is quadratically related to V_{cc}, voltage reduction yields the biggest savings in power consumption. As voltage reduction results in increased combinational logic delays [9], techniques such as pipelining and parallelism are employed for maintaining a constant throughput of the design. In addition, optimizations such as reduced algorithmic complexity, re-ordering of arithmetic expressions, word-length reduction can markedly reduce the overall capacitance and node switching activity in the design, thereby reducing the power-dissipation (detailed description is provided in [9, 23]). At the circuit level, clock-disabling techniques that turn off idle functional units can be exploited to extract further power savings.

5.2 Power reduction methodologies

5.2.1 Reduction in arithmetic complexity

The computationally most intensive operation involved in the RAKE receiver is the correlation operation where the sampled complex multi-path receiver data is correlated with the

spreading waveform vector for the user and pilot channels. For the p^{th} finger, the correlation output $X^p_{cor}(i)$ corresponding to the i^{th} signaling interval can be represented by,

$$X^p_{cor}(i) = \int_{iT+\tau_p}^{(i+1)T+\tau_p} r(t)s_1(t - iT - \tau_p)dt \tag{5.2}$$

where $s_1(t) = \sum_{n=0}^{N-1} c_k(n)g_T(t - nT_c) = (\sum_{n=0}^{N-1} c_k(n)\delta(t - nT_c)) \otimes g_T(t)$. When implementing the correlation operation as a digital matched filter, the complexity of the correlation operation is governed by the length of the signature waveform vector N_{corr} and the number of active fingers P. The signature waveform vector $\mathbf{s}_{1,p}$ is represented by the discrete-time convolution of the length N spreading sequence $\{c_1(n)\}$ and the M tap raised cosine filter with impulse response $\{g_T(n)\}$. The square-root raised cosine filter is given by $M = 2DS + 1$ taps (being linear phase) where D is the group delay of the filter and S is the upsampling rate at the filter input. The length of the convolution output is given by $N_{conv} = M + NS - 1$ samples. Assuming values of $D = 10$ samples, $S = 2$ samples/chip, we obtain $M = 41$, $N_{conv} = 2N + 40$ samples, hence the overall correlator length is specified by $N_{corr} = N_{conv}$. For a spreading code of length $N = 32$, $P = 3$ path channel, $L = 16$ tap channel estimator (as per Table 3.1 in Chapter 3), the arithmetic complexity of the RAKE receiver with ideal correlation equals $16NP + 318P + 2LP - 1 = 2585$ flops/symbol. We explore the reduction in the correlator length as a means for achieving reduction in arithmetic complexity. We consider the following two schemes:

- **Sampling at 2 samples/chip**: The starting and ending $DS = 20$ samples of the spreading waveform at the convolution output occur due to the group delay of the filter $g_T(n)$. By discarding these $2DS = 40$ samples and retaining the steady state response, the correlator length reduces to $N_{corr} = N_{conv} - 40 = 2N$ samples/symbol, which translates into savings in arithmetic complexity. Thus the number of correla-

tion operations involved in the pilot correlators (for channel estimation) and rake correlators (for despreading and detection) are reduced by $320P = 960$ flops/symbol to 1625 flops/symbol. In Chapter 6, the performance of the resulting receiver (with truncated correlation waveform) is shown to be almost identical with that obtained with perfect correlation. We call this receiver as the *reference RAKE receiver*.

- **Sampling at 1 sample/chip**: To achieve a reduction in the arithmetic complexity, we reduce the sampling rate for the despreading operation in the RAKE correlators to 1 sample/chip, and investigate the resulting complexity vs. performance tradeoffs. This halves the length of the correlator for the RAKE despreading operation to $N_{corr} = N$ samples/symbol and a corresponding reduction in the overall flop count by $4NP = 384$ flops/symbol to 1241 flops/symbol. As the performance of detection is heavily influenced by the accuracy of channel estimates, the pilot channel correlation is still performed at 2 samples/chip. The complexity reduction comes at the tradeoff of reduced correlator output energy owing to the halved correlation length. In Chapter 6, we demonstrate a significant power reduction with acceptable detection performance due to this optimization. We call this receiver as the *reduced complexity RAKE receiver*.

Impact on Clocking frequency

For the reference implementation of the DS-CDMA RAKE receiver, the architecture employed a uniform clock domain throughout the design. Since the implementation is a wholly parallel implementation, all the fingers in the PILOT and RAKE correlators begin and end their correlation simultaneously. In a practical implementation of the reduced complexity DS-CDMA RAKE receiver, the halving in the input sampling rate to the RAKE

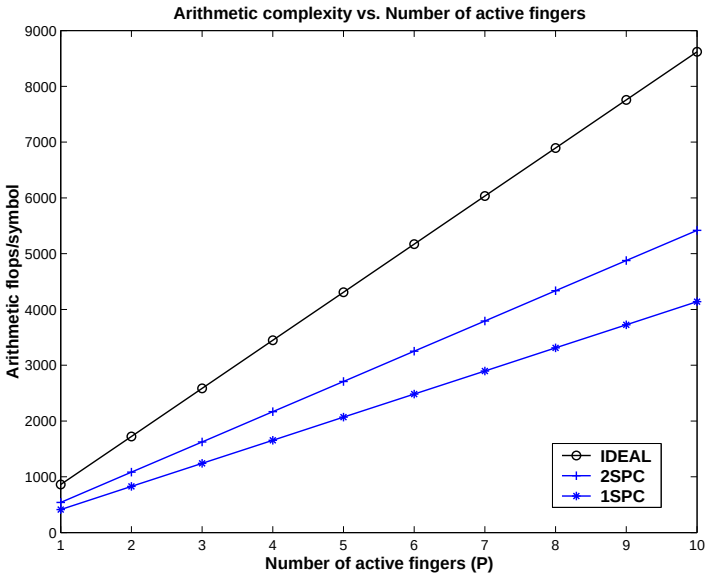

Figure 5.1 : Arithmetic complexity (flops per symbol demodulation) for ideal, reference, and reduced complexity RAKE receivers in DS-CDMA downlink

despreading unit would imply that the RAKE correlation would complete twice as fast as the PILOT correlation. This means that the RAKE correlator would remain idle for half the symbol duration, and still be clocked by the sample-rate clock, resulting in wasteful dissipation of idle clocking power. Therefore, the clock input for the RAKE correlation network is derived from the global clock at half the input sampling rate. Note that the reduced clocking rate *does not* reduce the effective symbol rate of the system.

5.2.2 Word-length reduction

Overview

Word-length reduction can help achieve significant gains in any design with regard to increased speed, area occupancy and power consumption. The principal gains obtained from word-length reduction come from three principal reasons [9]. Firstly, the reduced precision reduces the average activity of the entire design resulting in fewer switching events and

consequently lower power consumption. Secondly, functional operations such as multiplication and addition can be run much faster. As a consequence, the supply voltage can be reduced while keeping the throughput constant. This technique is very effective in custom CMOS ASIC circuits where standard cell libraries can be “tuned” for running at a particular voltage, while achieving the desired throughput. Lastly, the reduced precision implies that the effective load capacitance as seen by the heavily loaded lines (especially clock buffer lines) is significantly reduced.

Reduced Precision in the DS-CDMA RAKE receiver

Prior to exploring power optimizations using word-length reduction for the DS-CDMA RAKE receiver, extensive fixed-point simulations were performed in a SystemC [3] environment to evaluate the numerical stability of the reference and reduced complexity RAKE receiver algorithm. A minimum word-length of 10 bits was required for the RAKE receiver to achieve acceptable performance(within 1 dB) of the floating point version of the algorithm (this will be discussed further in the next chapter highlighting the results). The implementations of the reference and reduced complexity RAKE receivers (performed on the Virtex-II FPGA) were made parametrized, so that the precision requirements of the entire design could be changed “off-line” with minimal modifications.

5.2.3 Clock-gating

Overview

The global clock distribution network can consume anywhere between one-quarter to one-half of the active power in a synchronous design [30]. The reason for this is that the global clock signal drives a large load capacitance, and switched at every clock cycle. To give a simple example, the on-line clock power consumption in a design employing a 50

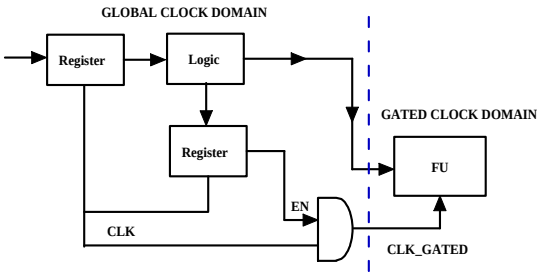

Figure 5.2 : A generic scheme for employing clock-gating

MHz clock having a load capacitance of 10 nF (typical values for a large design) at an operating voltage of $V_{cc} = 1.5$V equals 1.125 watts! This is an unacceptably large value for systems having strict power-constraints such as hand-held applications. Clock-gating is a simple yet powerful technique that can achieve significant reduction in the dynamic clocking power consumption by selectively disabling the clock to portions of the design that are functionally inactive.

Conceptually, the idea is to gate the clock with a control signal that is low during the period of inactivity and high otherwise. Figure 5.2 shows the generic description of a clock gated system. FU represents the functional unit that may be running at a substantially reduced rate compared to the rest of the system. Since FU has prolonged periods of inactivity, the clock distribution network serving FU can be turned off, during the idle durations. In order to generate the appropriate clock CLK_GATED, an enable signal EN is generated synchronously with the global clock CLK. The gated clock CLK_GATED is the logical AND operation of CLK and EN. During the period when FU is active, $EN = 1$, therefore $CLK\_GATED = CLK$. For the rest of the time, EN is held low and $CLK\_GATED = 0$.

Thus, the design is now partitioned into two separate domains as shown in the figure by the dashed line. For reliable operation of the gated clocking domain, CLK_GATED

should be hazard free. Otherwise, any spurious glitches in the enable signal EN will be propagated to FU when $CLK = 1$. Further, the addition of clock gating adds skew to the gated signal CLK_GATED with respect to CLK. If the size of the functional unit FU is large, there may be timing violations resulting from unequal timing arrivals of CLK_GATED to different parts of FU. In spite of these drawbacks, a carefully planned and well-thought design will try to minimize the resulting skew and ensure almost identical clock arrival times for the gated clock throughout FU.

Exploiting Clock-gating for the DS-CDMA RAKE receiver

During the i^{th} symbol interval, the computation of the complex channel coefficients $\mathbf{h}_i$ and the coherent maximal ratio combining operation occur at the symbol rate namely $f_{sym} = \frac{1}{T_b} = \frac{f_{samp}}{NS}$. Therefore, the clock-gating technique was employed to disable the clock distribution to the channel estimation and maximal ratio combining block, as long as the despreading operation for the i^{th} symbol was incomplete, and enable the clock duration during their active phase.

5.3 Architectural implementations

To quantify the effect of the aforementioned methodologies, architectures incorporating the power saving techniques were implemented on a Virtex-II FPGA. Four distinct implementations were considered in this thesis. They are enumerated below:

- **Reference architecture**: Figure 5.3 shows the reference architecture of the RAKE receiver. This implementation employs a uniform input sampling rate of 2 samples/chip for both the PILOT and RAKE correlator matched filtering operations. The external clock is passed through a delay-locked loop to derive the global clock buffer

CLK running at the input sample frequency of $f_{samp} = 24.576$ MHz.

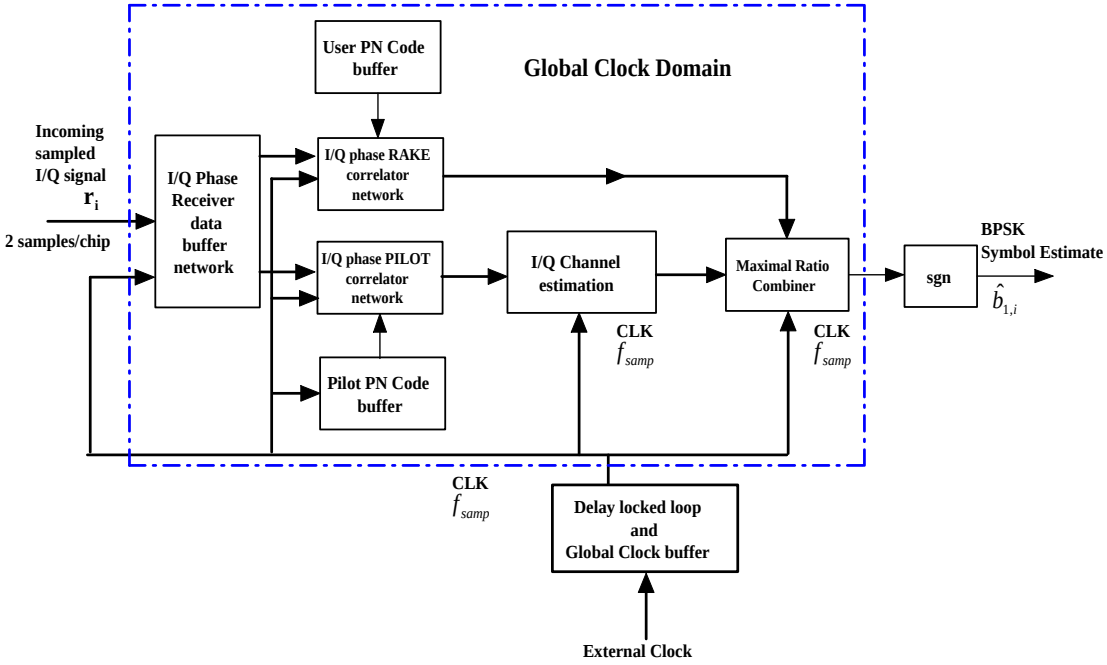

Figure 5.3 : Architecture of the reference DS-CDMA downlink RAKE receiver

- **Reduced Complexity architecture**: To explore the effects of reduced arithmetic complexity on the resulting power consumption of the RAKE receiver, the wide-band signal was input at the rate of 2 samples/chip to the PILOT correlator and 1 sample/chip to the RAKE correlator. Figure 5.4 shows the architecture of the resulting reduced complexity RAKE receiver with two separate clocking domains namely CLK (shown by the solid box) and CLK_DV (shown by the dashed box) running at $f_{samp} = 24.576$ MHz and $\frac{f_{samp}}{2} = 12.288$ MHz respectively. While the global clock buffer distribution CLK was used to clock the PILOT matched filtering operation, the second clock buffer CLK_DV was used to clock the RAKE matched filtering, channel estimation and Maximal Ratio Combining blocks. The presence of two in-

dependent clocking domains required the use of additional synchronizing logic to transfer signals (such as the pilot soft matched filter output) from the CLK domain to CLK_DV domain. Further, separate state machines were encoded in order to describe the control logic for operation of each of these domains.

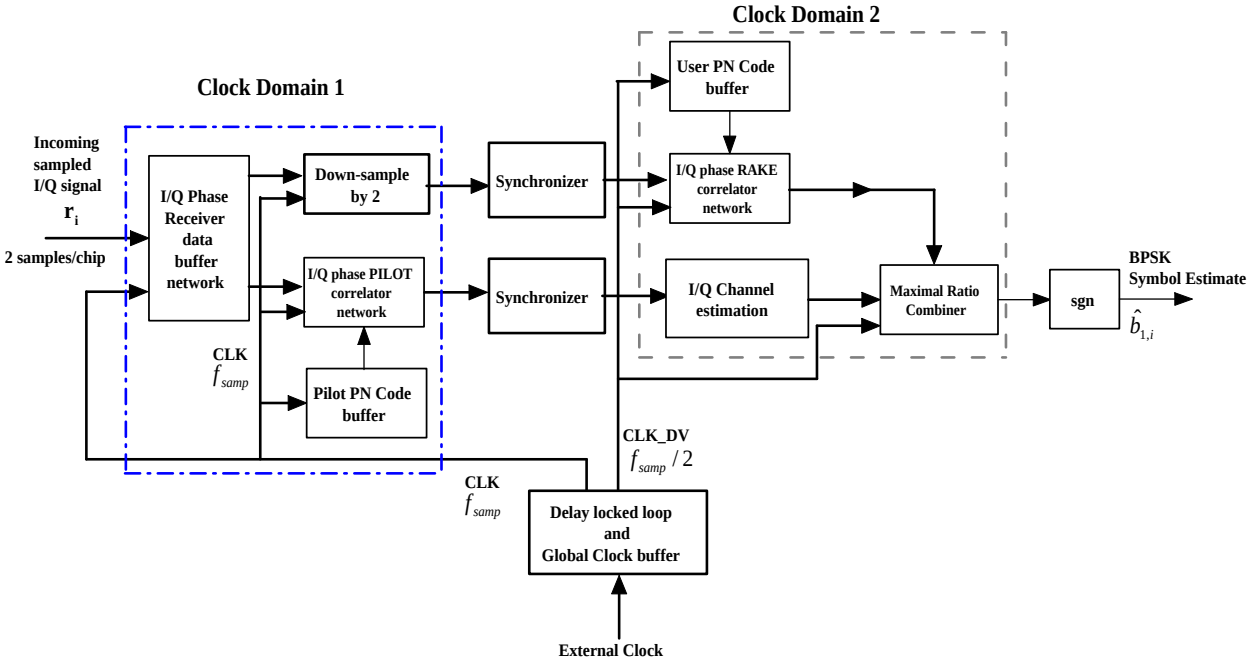

Figure 5.4 : Architecture of the DS-CDMA downlink RAKE receiver with reduced complexity

- **Reference architecture with Clock-gating**: To facilitate power reduction by disabling the clock distribution network to the idle functional units, the reference architecture was modified to accommodate a gated clock for performing the operations of channel estimation and Maximal Ratio combining. Figure 5.5 shows the architecture of the reference RAKE receiver with clock-gating features. The gated clock CLK_GATED is derived from the global clock buffer CLK and used to disable the clocking distribution to the channel estimator and Maximal Ratio Combiner unit

during their idle duration.

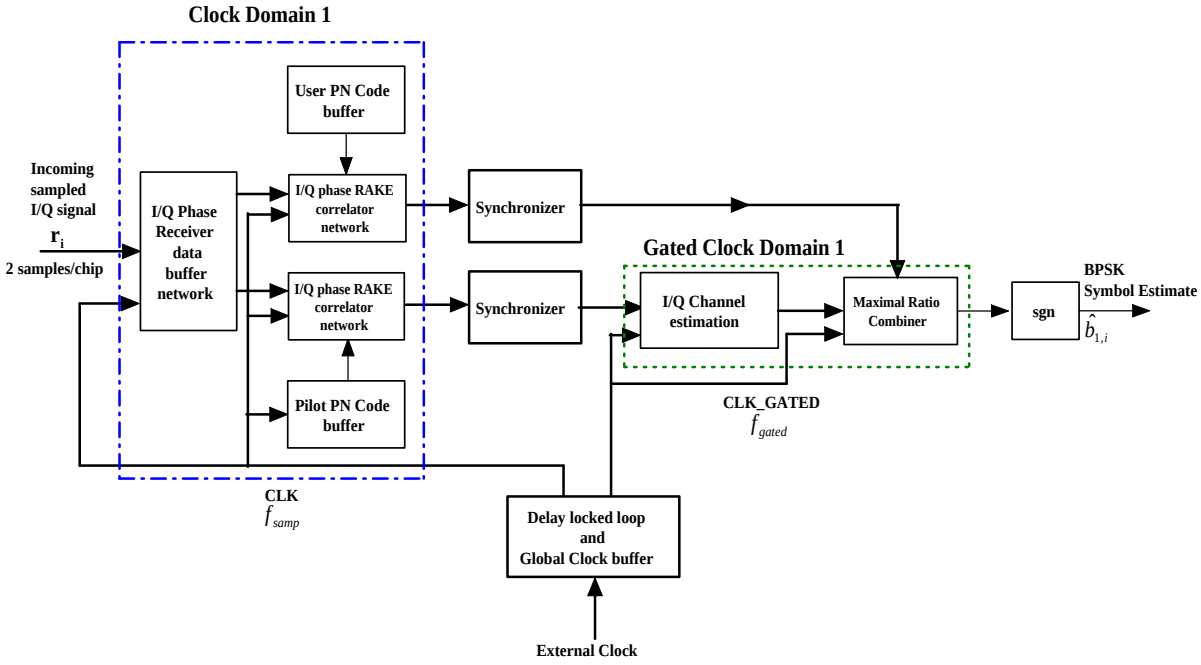

Figure 5.5 : Architecture of the reference DS-CDMA downlink RAKE receiver with clock-gating

- **Reduced complexity architecture with Clock-gating**: The fourth architecture incorporated clock gating into the reduced complexity DS-CDMA RAKE receiver architecture. Figure 5.6 shows the resulting architecture. Four distinct clocking domains were required, in order to implement this architecture. While CLK and CLK_DV formed the global clock domains, the gated clocks namely CLK_GATED and CLK_DV_GATED were derived from these domains. While deriving the gated clocks, care was taken to ensure that the logic skew between the global clocks and the gated clocks was kept minimum. While CLK was used to clock the PILOT matched filtering operation (at 2 samples/chip), CLK_DV was used to clock the RAKE matched filtering (at 1 sample/chip). The gated clock CLK_GATED was

used to clock the channel estimation operation, which takes in the narrow band output of the PILOT matched filtering operation. The maximal ratio combining operation, which takes in the narrow band output of the RAKE matched filtering operation and the channel estimates, was clocked with the gated clock CLK_DV_GATED.

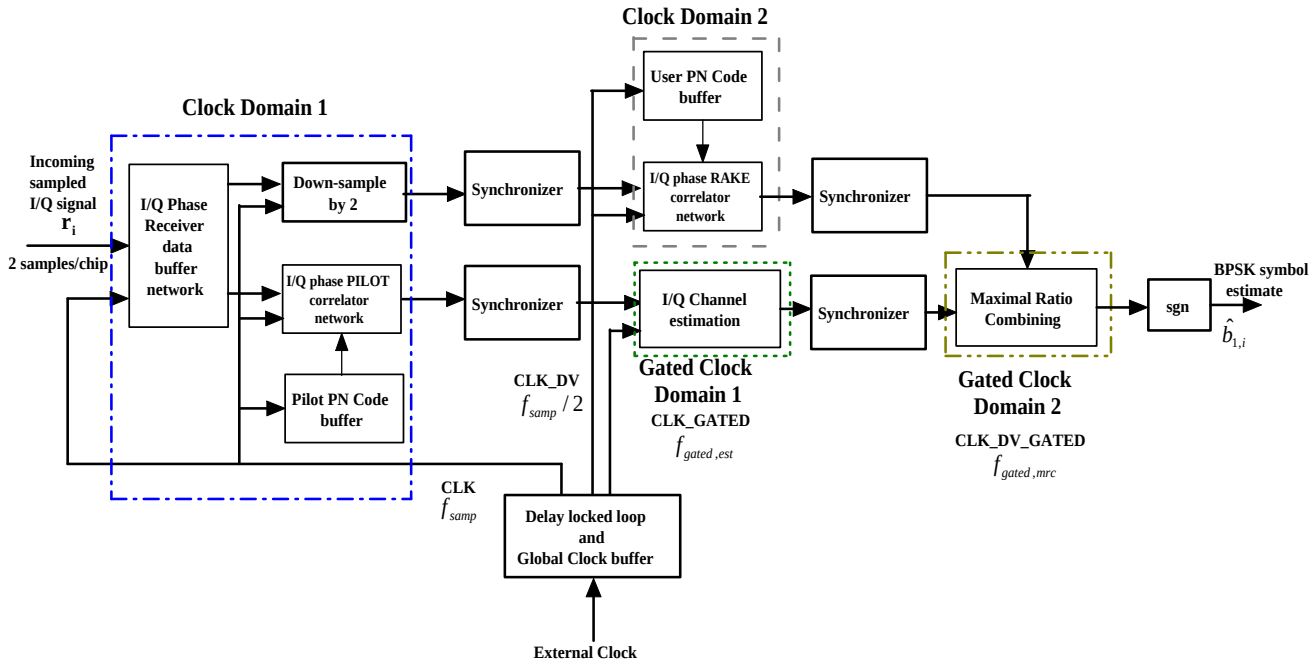

Figure 5.6 : Architecture of the DS-CDMA downlink RAKE receiver with reduced complexity and clock-gating features

Each of the above architectures were realized for varying input sampled precision of 16, 14, 12 and 10 bits respectively. We describe the performance and power-consumption of the above receivers in the next chapter.

Chapter 6

Results

6.1 Algorithm Performance Analysis

The simulation parameters were chosen as per the specifications given in Table 3.1 in Chapter 3. All the users were assigned unit transmit amplitudes. An additional code-multiplexed pilot channel with a 3 dB higher power was employed for channel estimation at the mobile receiver. The complex multi-path coefficients were generated to have a zero mean and unit variance. The oversampling rate at the transmitter and receiver front end was chosen to be 2 samples/chip in order to account for fractional multi-path delays. The A/D converter at the receiver front end was chosen to have an 8 bit width ($S8Q7$ format). We consider the performance of the following DS-CDMA RAKE receivers:

- Reference RAKE receiver performing truncated correlation sampled at 2 samples/chip (Complexity=$16NP - 2LP - 2P - 1$ flops/symbol).
- Reduced arithmetic complexity RAKE receiver performing truncated correlation sampled at 1 sample/chip for detection and 2 samples/chip for channel estimation (Complexity=$12NP - 2LP - 2P - 1$ flops/symbol).

The performance of these receivers were compared against a DS-CDMA RAKE receiver employing perfect correlation(highest complexity of $16NP+318P+2LP-1$ flops/symbol). Two metrics were chosen in order to quantify the performance of the algorithms. First, the average received $SNR = 10\log_{10}(\frac{E_b}{N_0})$ was varied (refer Equation 2.6 in Chapter 2) to

study the effect on the Bit-error rate performance of the algorithm. Next, the performance of the algorithm in the presence of multi-access interference (MAI) was evaluated by varying the number of interfering users for a fixed $SNR = 10$ dB.

6.1.1 Single-user, Single-path fading channel

We consider a 1 user, 1 path DS-CDMA downlink system in order to characterize the performance of the aforementioned receivers in the absence of interferers and multi-paths. The channel coefficients were drawn from an uncorrelated Rayleigh fading distribution. Perfect channel knowledge was assumed at the receivers. For reference, these curves are plotted against the lower theoretical bound on error probability for the RAKE receiver in a single path Rayleigh fading channel given by $P_{err} = \frac{1}{4\gamma}$ where $\gamma = \frac{E_b}{N_0}$ is the average received SNR (note that E_b is the average received energy per bit). The results were obtained after averaging the output obtained after 40 simulation runs per data-point of 1000 transmitted symbols.

Floating point performance

In the first set of simulations, we consider the floating point performance of the matched filter receivers (infinite precision). All computations are performed with full precision with no loss in accuracy owing to quantization errors. The results are shown in Figure 6.1. The performance of the matched filter receivers with perfect correlation("Ideal") and truncated correlation at 2 samples/chip ("2spc") is seen to be identical. Further, the error rates agree closely with the theoretically predicted lower bound ("Theory") which is an approximation for low SNR's. The performance of the matched filter receiver performing correlation at 1 sample/chip ("1spc") is seen to be satisfactory with an error rate of 0.5% at 20 dB SNR. The 2 dB degradation in performance can be explained by the decreased correlation out-

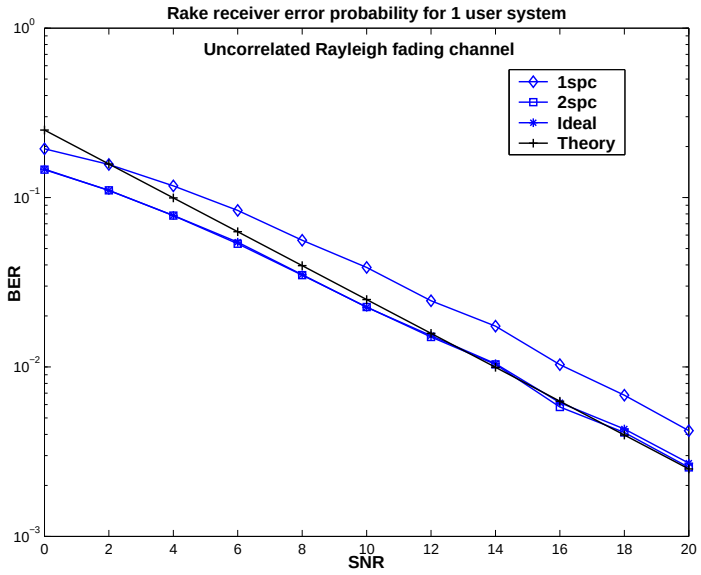

Figure 6.1 : Error Probability vs. Average SNR for DS-CDMA matched filter receivers.

put energy on account of the reduced arithmetic complexity. However, this degradation is perfectly tolerable since the detection is typically followed by decoders such as the Viterbi/Turbo algorithms which can achieve lower error rates in the order of $10^{-6} - 10^{-7}$.

Fixed point analysis

We consider the performance of the aforementioned matched filter receivers employing finite precision arithmetic. All fixed-point simulations were performed using the fixed-point classes provided by SystemC [3]. The results of all intermediate computations were truncated and saturation was employed for handling intermediate overflows. First, the performance of the reference matched filter receiver employing truncated correlation at 2 samples/chip is shown in Figure 6.2. The internal precision has been varied from 16 bits to 8 bits. For comparison, we have also simulated the matched filter receiver employing floating point with/without an A/D converter in the front end, and the predicted lower bound

in error probability. Next, the performance of the reduced arithmetic complexity matched filter receiver employing correlation at 1 sample/chip is shown in Figure 6.3.

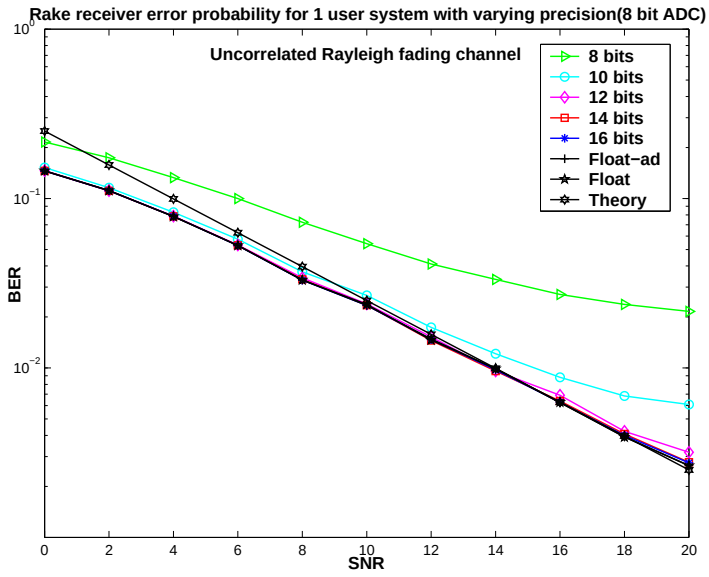

Figure 6.2 : Error Probability vs. Average SNR for Reference DS-CDMA RAKE receiver (single user).

Next, the performance of the reduced arithmetic complexity matched filter receiver employing correlation at 1 sample/chip is as shown in Figure 6.3.

We note that the fixed-point performance of both the reference and reduced complexity receivers is almost identical to the corresponding floating-point performance up to a 12 bit precision indicating the suitability of fixed-point arithmetic based architectures. Even at a 10 bit precision, the performance degradation is less than 1 dB up to $SNR = 16$ dB. At a 8 bit precision, the effect of quantization is clearly seen with a $4 - 5$ dB loss in performance compared to floating point.

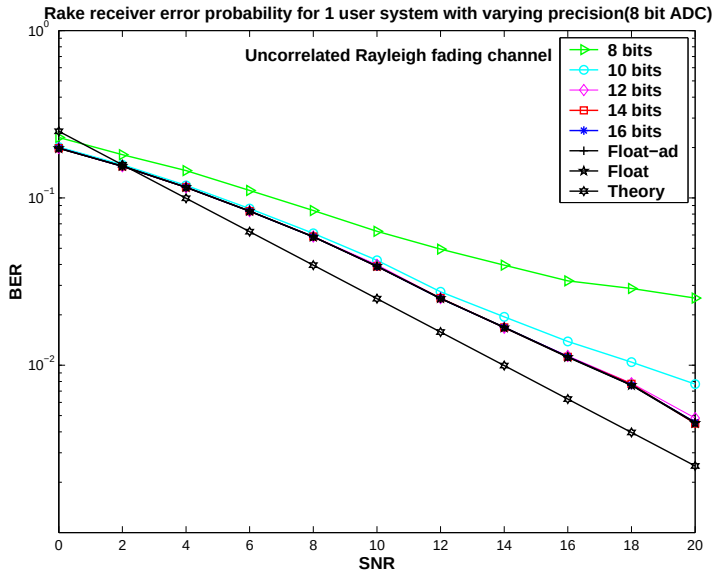

Figure 6.3 : Error Probability vs. Average SNR for Reduced Complexity DS-CDMA RAKE receiver (single user).

6.1.2 Multi-user, Multi-path fading channel

Based on the results shown in the single user, single path case, we describe the performance of the reference and reduced complexity RAKE receivers for a multi-path channel in the presence of interferers. The simulations assume a 5 user, 3 path correlated Rayleigh fading channel based on the Jakes mobility model. For each data-point, 40 separate simulations of 5000 transmitted bits were carried out. The multi-path delays were fixed for each simulation and varied from one simulation to the next.

Figures 6.4 and 6.5 show the performance of the reference DS-CDMA RAKE receiver for the above scenario. We notice that the receiver performance in fixed-point is close to the ideal floating point performance, with negligible performance degradation up to a 12 bit precision. A marginal performance loss of 2 dB is observed with the 10 bit data-path.

Figures 6.6 and 6.7 show the performance of the reduced complexity DS-CDMA RAKE receiver. Like the single-user, single-path case, the reduction in complexity causes a per-

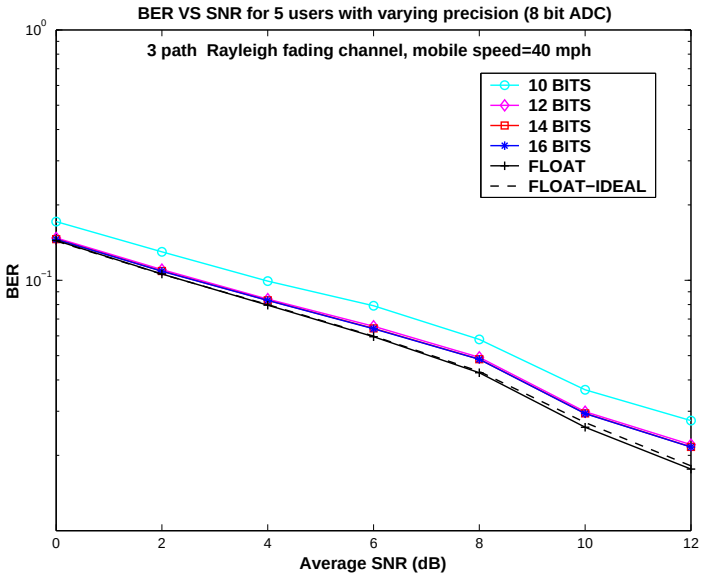

Figure 6.4 : Error Probability vs. Average SNR for Reference DS-CDMA RAKE receiver (multi-user).

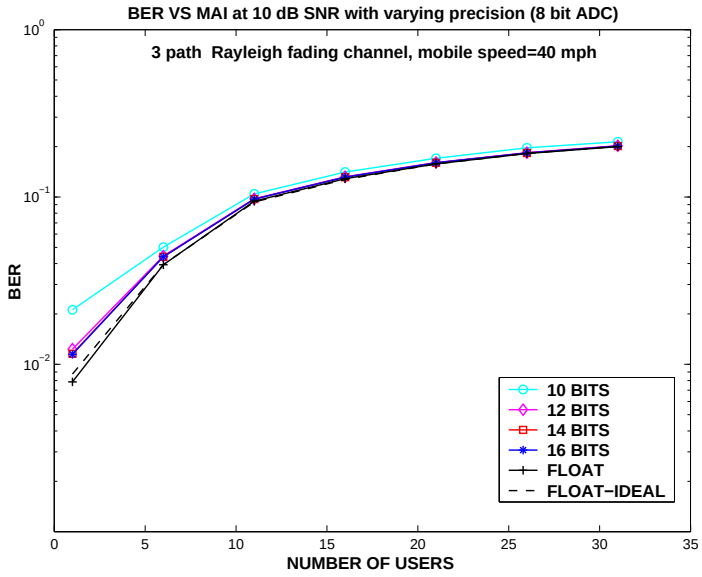

Figure 6.5 : Error Probability vs. Multi-access interference for Reference DS-CDMA RAKE receiver.

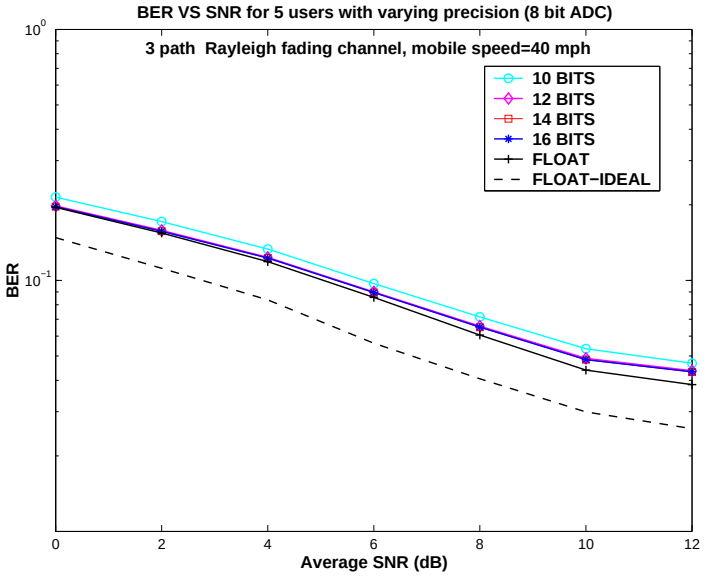

Figure 6.6 : Error Probability vs. Average SNR for Reduced Complexity DS-CDMA RAKE receiver (multi-user).

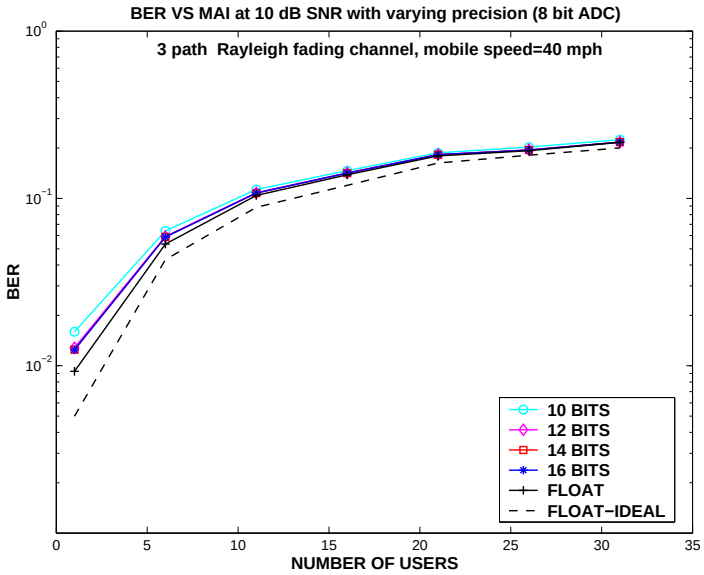

Figure 6.7 : Error Probability vs. Multi-access interference for Reduced Complexity DS-CDMA RAKE receiver.

formance drop of 2 dB compared to the ideal DS-CDMA RAKE receiver employing ideal correlation (shown by the dashed line in black). As shown in the following section, we assert that this performance degradation is perfectly acceptable considering the savings in power dissipation as a result of the reduced complexity. Again, we note that the receiver performance in fixed-point is almost identical with the floating-point performance up to a 10 bit precision.

6.2 Results of FPGA implementation

As mentioned in the previous chapter, four different architectures for the RAKE receiver were targeted for a 2 million gate Virtex-II (XC2V2000 series) FPGA, which employs a supply voltage of $V_{cc} = 1.5$ V. Synthesized complex receiver data for an urban 3 path Rayleigh multi-path channel was passed through each receiver implementation, and symbol detection was carried out. The results of each simulation were corroborated with the corresponding SystemC/MATLAB simulation to verify correctness of performance.

6.2.1 Timing simulation

For finding the dynamic power consumption in the design, the synthesized receiver data was run through the receiver. An external clock running at 50 MHz was produced to clock the receiver. * The analysis was carried out following the synthesis, translation, mapping, netlist extraction, and the post-placement and routing phase. Extensive timing simulations were carried out in the Modelsim [2] simulator to model true-device behavior. All internal node transitions occurring during the course of the simulations were dumped into a

*Since the recommended clocking speed of the Virtex-II FPGA is at least 26 MHz, the timing simulations were carried out at a clocking frequency of 50 MHz. The observed results are scaled to the sampling rate of $f_{samp} = 24.567$ MHz for a data rate of 384 kbps.

".vcd" (Value-Change-Dump) file format. The .vcd files were then analyzed by the power analysis tool XPower [1] provided by Xilinx [7]. A power report was generated as a result of the analysis that contained the overall power consumption, as well as a summary of the dominant power consumption among the individual blocks of the design. Finally, the dynamic power consumption was obtained after calculating the difference of the overall design power consumption and the queiscent power (225 mW) of the FPGA. [†]

6.2.2 Power estimation for clock-gated architectures

For the architectures employing clock-gating, an indirect method was used to estimate the dynamic power consumption of the receiver. The reason for this approach was that XPower lacked the capability to estimate the activity rate of gated clocks in its current version. Therefore, the power estimation for the clock gated architecture was performed by adding the data-path power consumption of the corresponding ungated architecture and the clocking power of the clock gated architecture, given by,

$$P_{dyn,gated} = \underbrace{(P_{dyn,ungated} - P_{clock,ungated})}_{\text{Data-path power}} + \underbrace{P_{clock,gated}}_{\text{Clocking power}} \tag{6.1}$$

where $P_{dyn,gated}$ represents the dynamic power dissipation of the clock-gated architecture, $P_{dyn,ungated}$ represents the dynamic power dissipation of the corresponding ungated architecture, and $P_{clock,ungated}$, $P_{clock,gated}$ represent the clocking power dissipation of the respective architectures. $P_{dyn,ungated}$ and $P_{clock,ungated}$ were known from the power analysis obtained from timing simulations of the ungated architectures, while $P_{clock,gated}$ was estimated since the percentage toggle time, and the capacitive loads of the gated clock were

[†]The queiscent power (Q-Power) of a FPGA is fixed by the FPGA area, internal operating voltage and independent of the size of the design. The Virtex-II FPGA has a Q-Power specification of 225 mW at an operating voltage of $V_{ccint} = 1.5$ V.

known before-hand.

6.2.3 Power dissipation of receiver architectures

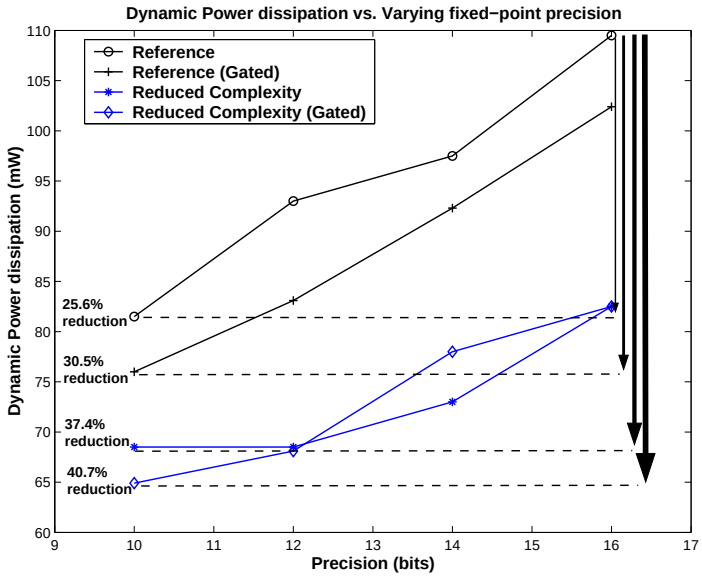

Figure 6.8 : Dynamic power dissipation vs. Varying fixed-point precision of different DS-CDMA mobile RAKE receiver architectures

Figure 6.8 illustrates the variation in dynamic power dissipation with precision for the DS-CDMA RAKE receiver, obtained for the reference implementation, reduced complexity implementation, and the corresponding clock-gated architectures. All the reported power-savings are calculated with respect to the 16-bit reference DS-CDMA RAKE receiver architecture, and incorporate the influence of reduced precision *and* power-saving methodology specific for that architecture (reduced complexity/clock gating). For each of the four architectures, we notice a clear trend with the 10 bit data-path achieving the lowest power. The maximum power-savings of 40.7% are obtained for the 10 bit data-path implementation of the reduced complexity RAKE receiver with clock-gating of idle blocks.

In Table 6.1, the results of implementation of the reference and reduced complexity

architectures have been reported. The area shown in the table is represented in FGPA slices (refer Chapter 3) as well as the percentage occupancy in the FPGA, with the available area being 10752 slices in a Virtex-II FPGA. Considering *only* the effect of reduced precision, the reference architecture shows a power reduction of 25.6% for the 10 bit data-path compared to the 16 bit data-path. For the reduced complexity architecture, we observe power savings of 16.96% for the 10 bit data-path. These power savings are quite significant considering that the 10 bit data-path achieves almost close to the equivalent floating point performance for both the reference and reduced complexity receivers (performance loss being less than 1 dB).

Next, we consider the effect of complexity reduction on the resulting power savings. The 16 bit reduced complexity RAKE receiver achieves a power saving of 24.65% compared to the 16 bit reference RAKE receiver implementation. The combined effect of reduced precision and arithmetic complexity results in 37.4% reduction in dynamic power consumption for the 10 bit RAKE receiver (Figure 6.8). In the earlier results in Figure 6.3 and 6.6, we have observed less than a 2 dB loss in the performance of the reduced complexity RAKE receiver compared to the reference receiver. Clearly, the effect of reduction in arithmetic complexity and precision offers significant savings in power consumption with a favorable trade-off in performance.

Table 6.2 shows the effect of clock-gating of the channel estimation and Maximal Ratio Combining blocks on the resulting power consumption P_{dyn} of the receiver. The average area occupancy of the clock gated portions of the both the reference and the reduced complexity receivers is seen to be 35% of the overall design size.

For a 16 bit data-path, clock-gating leads to a power reduction of 6.45% in the reference RAKE receiver, while no power reduction is seen for the reduced complexity RAKE receiver. For the 14 bit data-path, the reduced complexity RAKE receiver actually shows

Type	Bits	Area (Slices)	P_{dyn} (mW)	Savings
Reference	16	3572(33%)	109.5	-
	14	3000(28%)	97.5	10.95%
	12	2341(22%)	93	15.06%
	10	1844(17%)	81.5	25.6%
Reduced Complexity	16	3724(35%)	82.5	24.65%
	14	3134(29%)	73	33.33%
	12	2457(23%)	68.5	37.44%
	10	1942(18%)	68.5	37.44%

Table 6.1 : FPGA implementation of Reference and Reduced Complexity architectures for the DS-CDMA downlink RAKE receiver

increased power dissipation (78.01 mW with clock-gating against 73 mW without clock-gating). The reason for this counter-intuitive observation is that the FPGA based implementation of the clock-gated design requires the use of additional clock-distribution networks for maintaining uniform clock arrival times of the gated clocks throughout the design. The operation of these buffers consumes additional power leading to reduced benefits incurred by the clock-gating technique. As the reduced complexity RAKE receiver with clock-gating employs 2 gated clocks (as compared to only 1 gated clock for the reference RAKE receiver with clock-gating, see Chapter 5 for the architectures), there is an increased overhead in the clock distribution which actually causes the higher power consumption with the clock-gating.

To investigate the impact of clock-gating without the clock distribution overhead, the power consumption of the clock gated design in the ideal case $P_{dyn,ideal}$ is also highlighted.

Type	**Bits**	**Area (Slices)**	**Gated Area (Slices)**	P_{dyn} **(mW)**	**Savings** $(\%)$	$P_{dyn,ideal}$ **(mW)**
Reference (clock-gated)	16	$3571(33\%)$	1242	102.43	6.45%	100.59
	14	$2999(27\%)$	1045	92.33	15.68%	90.49
	12	$2340(22\%)$	818	83.16	24.05%	81.33
	10	$1843(17\%)$	645	76.06	30.53%	74.23
Reduced Complexity (clock-gated)	16	$3678(34\%)$	1236	82.5	24.65%	77
	14	$3094(29\%)$	1039	78.01	28.76%	72.5
	12	$2423(23\%)$	812	68.13	37.78%	62.62
	10	$1914(18\%)$	645	64.96	40.67%	59.44

Table 6.2 : FPGA implementation of Reference and Reduced Complexity architectures (with clock-gating) for the DS-CDMA downlink RAKE receiver

Such a scenario can be considered in the case of an ASIC where the overhead due to the dedicated clock distribution network is eliminated. Without the overhead of the clock distribution network, we observe clock-gating leads to additional savings of 2 mW for the reference RAKE receiver (having 1 active and 1 gated clock domains) and 5.5 mW for the reduced complexity RAKE receiver (having 2 active and 2 gated clock domains).

Finally, we consider the combined effect of clock-gating and precision reduction on the power dissipation of the architectures. The 10 bit data-path implementation of the clock-gated reference RAKE receiver achieves the highest reduction of 30.5% in power dissipation, while the clock-gated reduced complexity RAKE receiver achieves a 40.7% reduction, compared to the 16 bit data-path implementation of the reference RAKE receiver. In the ideal case, the corresponding savings are 32.3% and 45.71% respectively.

Chapter 7

Conclusions and Future Work

In this work, we have examined design methodologies for reducing the online power dissipation in a DS-CDMA mobile RAKE receiver. The design methodologies have been targeted at the different stages of the VLSI design cycle namely the algorithm design, architecture design, and the circuit design phase. At the algorithm level, reduction in arithmetic complexity has been investigated for obtaining savings in the dynamic power dissipation. At the architectural level, precision reduction and clock-gating methodologies have been exploited for additional savings.

Reduction in precision shows that a 10 bit data-path achieves near floating point performance with minimal performance degradation for the reference RAKE receiver. Power-optimized architectures based on a Xilinx Virtex-II FPGA have been proposed for implementing both the conventional and reduced complexity DS-CDMA RAKE receiver. Simulation results indicate that power reduction of up to 37.44% can be achieved by a 10 bit reduced complexity RAKE receiver, with a performance degradation of less than 2 dB, constituting a favorable performance vs. power trade-off. Clock-gating based techniques have also been explored to disable the clock distribution to idle functional units such as the channel estimation and maximal ratio combining blocks. These approaches yield a power reduction of 30.53% in the reference RAKE receiver and 40.67% in the reduced complexity RAKE receiver.

In future, we would like to incorporate multi-path delay estimation into the architecture of the receiver. The initial delay acquisition and synchronization phase are very compu-

tationally expensive, hence it is important to optimize them for power consumption. An interesting optimization is to replace the bank of P dual ported SRAM memories (where P is the number of fingers) in the receiver front end with a single dual ported memory to feed appropriately delayed receiver data to individual fingers. There is further scope for reducing the computational cost involved in the correlation operations. In this thesis, we have assumed that the matched filtering is performed at the sample rate by correlating the sampled received signal with the truncated spreading sequence waveform of the user at 1 or 2 samples/chip. The matched filtering phase can be broken down into an initial chip-matched filtering phase, and a despreading phase. The chip-matched filter would yield reliable chip-estimates to both the RAKE and PILOT correlators. By doing so, the number of multiplication operations involved would be greatly reduced since both the RAKE and PILOT correlators would now be performing despreading with a $\{-1, +1\}$ sequence. Moreover, techniques such as distributed arithmetic based filtering could be employed for performing chip-matched filtering, thus avoiding the need for explicit multiplications. This would result in considerable power savings. Finally, it would be interesting to optimize the performance and power consumption of these receivers in the context of multiple transmit/receive antenna systems.

Bibliography

[1] FPGA Xpower tutorial. Available from http://support.xilinx.com/ support/techsup/tutorials/tutorials4.htm.

[2] Modelsim Xilinx User's Manual. Available from http://www.model.com.

[3] Open SystemC Initiative. Available from http://www.systemc.org/ projects/systemc.

[4] Overview of the FPGA. Available from http://www.vcc.com/fpga.html.

[5] Virtex-II Handbook. Available from http://www.xilinx.com/products/virtex/ handbook/index.html.

[6] Why Floating Point DSP? Available from http://www.ipitec.it/.

[7] Xilinx home page. http://www.xilinx.com.

[8] R. Baghaie and T. Laakso. Implementation of Low Power CDMA RAKE receivers using strength reduction transformation. In *Proceedings of IEEE Veh. Technol. Conf*, pages 543–548, Saint Louis, MO, May 1991.

[9] A.P. Chandrakasan, M. Potkonjak, R. Mehra, J. Rabaey, and R.W. Brodersen. Optimizing power using transformations. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 14(1):12–31, January 1995.

[10] K.C. Chang. *"Digital Design and Modeling with VHDL and Synthesis"*. IEEE Computer Society Press, 1997.

[11] K.G. Cornett and S.B. Wicker. Bit error rate estimation techniques for Digital Land-mobile radios. In *Proceedings of IEEE Veh. Technol. Conf*, pages 543–548, Saint Louis, MO, May 1991.

[12] E. Dahlman, B. Gudmundson, M. Milsson, and J. Scold. UMTS/IMT-2000 based on W-CDMA. *IEEE Communications Magazine*, 39(9):70–80, September 1998.

[13] S. Denett. The CDMA2000 ITU-R RTT candidate submission (0.18). copyright Telecommunication Industry Association, 1998.

[14] R. Davis et al. A design environment for high-throughput low-power dedicated signal processing systems. *IEEE Journal of Solid State Circuits*, 37(3):420–430, March 2002.

[15] R. Fantaccci and A. Galligani. An efficient RAKE receiver architecture with pilot signal cancellation for downlink communications in DS-CDMA indoor wireless networks. *IEEE Transactions on Communications*, 47(6):823–827, June 1999.

[16] D. Garrett and M. Stan. Power reduction techniques for a spread spectrum based correlator. In *Proceedings of International Symposium on Low Power Electronics and Design*, pages 225–230, 1997.

[17] R.D. Gaudenzi, F. Giannetti, and M. Luise. The effect of signal quantization on the performance of DS/SS-CDMA demodulators. In *Proceedings of the Global Telecommunications Conference, 1994*, pages 994–998, 1994.

[18] M. Latva-aho and M.J. Juntti. LMMSE detection for DS-CDMA systems in fading channels. *IEEE Transactions on Communications*, 48(2):194–199, February 2000.

[19] D. Linerbarger, F.A. Abi Zeid, and A.R. Shrivastava. Dynamic Range Tool, 2000. Signal Processing Lab, Engineering and Computer Science Department, University of Texas, Dallas.

[20] T. Ojanperä and R. Prasad. *"WCDMA: towards IP Mobility and Mobile Internet"*. Artech House publications, 2001.

[21] R. Price and P.E. Green Jr. A communication technique for multipath channel. *Proc. IRE*, 46:555–570, March 1958.

[22] J.G. Proakis. *"Digital Communications"*. New York: McGraw-Hill, 1995.

[23] J.M. Rabaey and M. Pedram. *"Low Power Design Methodology"*. Kluwer Academic Publishers, 1996.

[24] S. Rajagopal, S. Bhashyam, J.R. Cavallaro, and B. Aazhang. Real-time algorithms and architectures for multiuser channel estimation and detection in wireless base-station receivers. *IEEE Transactions on Wireless-Communications*, 1(3):468–479, July 2002.

[25] T.S. Rappaport. *"Wireless Communications"*. New York: McGraw-Hill, 1986.

[26] S. Sriram, K. Brown, and A. Dabak. Low-power correlator architectures for wideband CDMA code acquisition. In *Conf. Record of 33rd Asilomar Conf. Signals, Systems and Computers*, pages 125–129, 1999.

[27] G.L. Stüber. *"Principles of Mobile Communication"*. Kluwer Academic Publishers, 1996.

[28] E. Telatar. Capacity of Multi-Antenna Gaussian Channels. *AT&T Bell Labs Internal Tech. Memo.*, June 1995.

[29] A.J. Viterbi. *"CDMA Principles of Spread Spectrum Communication"*. Addison Wesley, 1995.

[30] H. Yu and J. Cho. Low-power design and architecture. *IEEE Potentials*, 20:18–22, August 2001.