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Electrical Characterizations of LiNbO₃ Thin Films in a Metal-Ferroelectric-Semiconductor Capacitor

by

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A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE

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ABSTRACT

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A LiNbO$_3$ thin film Metal-Ferroelectric-Semiconductor capacitor is analyzed with various electrical characterization methods for studying the polarization switching and the thin film conduction behavior. The polarization density vs. electric field (P-E) curve shows that the remnant polarization is 16.85µC/cm$^2$ and the coercive field is 117.25 KV/cm when maximum applied field is 286.2KV/cm for a sinusoidal input waveform. The capacitance vs. voltage bias (C-V) curve further demonstrates that the polarization charge is the dominant charge in controlling the ferroelectric semiconductor interface property. The switching transient current curve from a dual polarity four pulses chain study (P-S) gives the switching time of the sample about 80-100ns. Current vs. voltage (I-V) curve is explained with a back-to-back Schottky barrier controlled conduction mechanism. These electrical characterization results demonstrate that LiNbO$_3$ is a promising candidate for a Metal-Ferroelectric-Semiconductor-Field-Effect-Transistor (MFSFET) non-volatile non-destructive memory application.
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Chapter 1

Introduction

Since the discovery of ferroelectricity in 1921\cite{1}, it has been a natural idea for scientists to use the two spontaneous polarization directions as the two values of the Boolean algebra for memory applications. However, the research in this area developed quite slowly because of several serious problems such as fatigue, imprint and aging. It was not until the late 1980s there came a tremendous progress in ferroelectric memory applications due to the achievements on thin film technology. Most of the research now focuses on three different memory structures: ferroelectric Dynamic Random Access Memories (FeDRAM), ferroelectric Nonvolatile Random Access Memories (FeNVRAM) and Metal Ferroelectric Semiconductor Field Effect Transistors (MFSFET)\cite{2}.

In FeDRAM structures, the ferroelectric material is used as the capacitor dielectric material. The information is stored as charges rather than in the polarization directions. For DRAM applications the capacitor area per cell is the main restriction for high-density applications. A lot of work has been done to increase the capacitor geometry factor, area vs. film thickness (A/d), such as by stacking and trenching. But these methods greatly increase the processing complexity and expense. The large dielectric constant of the ferroelectric material, which is normally from several hundreds to even thousands, has the advantage of allowing fabricating large capacitors while maintaining a simple capacitor structure. Panasonic\cite{2} has already produced a 16Mb FeDRAM made with barium strontium titanate (BST) and integrated it into an integrated circuit (IC) in digital
mobile phones. Bigger capacities FeDRAMs, as high as 256Mb, are reported to be coming soon\textsuperscript{[1]}.\n
In FeNVRAM, the ferroelectric material is still used in a capacitor structure but another "driving" line is added besides the "word" and the "bit" line\textsuperscript{[4]}. The information is written into the capacitor by the driving pulse and retained as the polarization charges even when the power is off. So it is a non-volatile memory. The read-out is accomplished by sensing the polarization current flowing through the capacitor when the memory cell is open. Commercial devices have already reached the smart card market\textsuperscript{[5]}.

However, both of these memory structures need additional circuits to either refresh the cell (FeDRAM) or restore the original information after read-out (FeNVRAM). In the 1970s several researchers proposed the idea of the metal ferroelectric semiconductor field effect transistor (MFSFET)\textsuperscript{[6]}, which should be an ideal candidate for a one-transistor memory cell. The schematic of the MFSFET is illustrated in Fig. 1.1. In this structure the ferroelectric thin film is used as the gate insulator for a field effect transistor. Information is written into the film based on the polarization directions, which are determined by a programming voltage pulse. The polarization charges at the interface of the ferroelectric film and the silicon control the channel conductivity. Thus "1" or "0" can be read out as different magnitudes of the channel current. So the MFSFET structure fulfills the non-volatile non-destructive read-out operation. Several materials have been reported for MFSFET application including PZT\textsuperscript{[7]}, BaMgF\textsubscript{4}\textsuperscript{[8]} and SBT\textsuperscript{[9]}.\n
LiNbO₃ has been one of the most intensely studied materials due to its unique combination of optical, acoustic, electrical and ferroelectric properties. It has only one polarization direction, which is along the (006) orientation, and the bulk spontaneous polarization density of 71µC/cm² is the highest among all known ferroelectric materials.

![Diagram](image)

**FIGURE 1.1 The Metal-Ferroelectric-Semiconductor-Field-Effect-Transistor**

These features are ideal for memory applications since the 1-d polarization can well define the stored information, and a larger polarization can produce a larger amplitude difference on read-out drain current[^10]. The high Curie temperature (1210°C) of LiNbO₃ and its stable chemical property offer a wide working temperature range. But its coercive field is quite big, about 300kV/cm, so it is hard to switch LiNbO₃. However, if LiNbO₃ is used in a thin film form, less voltage is needed to reverse the ferroelectric domain. Rost
et al.\textsuperscript{[11]} reported the first LiNbO\textsubscript{3} MFSFET in 1991, and several other papers\textsuperscript{[12, 13]} also have reported subsequent research on it. The prototype transistor successfully fulfilled the memory write and read operation. But the transistor array demonstrated a “cross talk” problem; i.e., selecting one cell will also switch its near neighbors. Also, the electrode was easy to ablate due to the large current density flowing through the large area electrodes and could not be used for long runs. A more detailed study of the LiNbO\textsubscript{3} switching properties is thus required.

The present research combines several electrical characterization methods to investigate the LiNbO\textsubscript{3} Metal-Ferroelectric-Semiconductor (MFS) structure. The thesis is organized according to the various characterization methods. Chapter 2 introduces theories in explaining the polarization vs. electric field (P-E) curve shape and discusses the Sawyer-Tower circuit for measuring the P-E curve. Chapter 3 looks at the switching dynamics of the ferroelectric material and its corresponding polarization transient behavior. Chapter 4 goes into the origin of the capacitance vs. voltage bias (C-V) hysteresis curve. Chapter 5 compares possible conduction mechanisms in the MFS structure for analyzing the dominant factor leading to the leakage current. Detailed experimental setups are also described in chapters 2, 3, 4 and 5. Chapter 6 summarizes and discusses the experimental results. The last chapter gives the conclusion and indicates several possible research directions in the future.
Chapter 2

Polarization Switching of Ferroelectric Materials

2.1 Polarization vs. electric field

The polarization vs. electric field (P-E) curve has been a useful diagnostic tool to study the polarization behavior since ferroelectricity was found. Though the idea of a ferroelectric dipole reversal is quite straightforward for explaining and understanding the ferroelectric switching phenomena, there is still no generally accepted theory that can successfully explain all experimental P-E hysteresis curves for different materials. In real ferroelectric materials the properties are strongly influenced by many factors such as the microstructures, defects, compositional inhomogeneity and external fields. Furthermore, in thin films the film thickness plays an additional role and sometimes may be the dominant factor in controlling the ferroelectric response. The ferroelectricity itself may disappear when the thickness reduces to several nanometers \(^2\).

In theory, if only one pure domain exists, the P-E curve will look like Fig. 2.1(a). There is a sharp change of P at the coercive field \(E_c\). However, the real P-E curve will look more or less like the one in Fig. 2.1(b), which corresponds to a multi-domain structure. Different models are proposed to interpret the observed P-E hysteresis curves. One of these \(^14\) is based on the Landau-Devonshire theory, in which a Gaussian distribution is used to describe the variation of the offset voltage due to the charged defects.
FIGURE 2.1 P-E curves of (a) a single domain and (b) multi domains
This offset voltage transforms the abrupt hysteresis into a "soft" hysteresis. In this theory the intrinsic film property determines the hysteresis curve shape. But in theory proposed by Smith [15], the shape of the curve is said to be originating from a non-switching dielectric layer. This layer exists at the interface of the ferroelectric film and the electrode. The compensating charges, which move only laterally within this layer, form a depolarization field given by \( E_d = -Pt/\varepsilon_d d \), where \( t \) and \( \varepsilon_d \) are the thickness and dielectric constant of the dielectric layer respectively. The slope of the curve, defined as the reciprocal of the slope of the measured curve, is given by

\[
\frac{\partial E}{\partial P} = \frac{t}{\varepsilon_d d} \tag{2.1}
\]

The loop will become more tilted when the ratio of \( t/d \) is increased. The idea of a dielectric layer is also proposed by Miller et.al. [16] in modeling the ferroelectric capacitor. The theoretical prediction and experimental results match quite well.

### 2.2 Measurement of the P-E curve

There are several methods for measuring P-E curves including the pulse switching, the constant current [17] and the Sawyer-Tower circuit [18] methods. Due to the limitations of different measurement methods, the derived P-E parameters such as \( E_c \) and \( P_r \) from
these measurements will differ a bit from each other. The most popular method is based on the Sawyer-Tower circuit. A schematic Sawyer-Tower circuit is illustrated in Fig. 2.2

![Sawyer-Tower circuit diagram](image)

**FIGURE 2.2** the equivalent circuit diagram of Sawyer-Tower circuit

The ferroelectric sample can be modeled as a combination of a normal linear capacitor $C_1$ and a polarization nonlinear capacitor $C_F$. The linear capacitance $C_1$ can be obtained from the C-V measurement. The nonlinear capacitance $C_F$ actually demonstrates the P-E relation of the sample. The sample's finite resistance can be simulated with a parallel resistor $R_p$ that can be obtained from I-V curve. When an AC source voltage such as a sinusoidal wave is applied on the sample, a charge displacement current consists of the above three parts will flow through the integrating capacitor $C_0$ that is given by
\[ i(t) = C_i \frac{d(V_i(t) - V_o(t))}{dt} + A \frac{dP(t)}{dt} + \frac{V_i(t) - V_o(t)}{R_p} \tag{2.2} \]

\( V_i(t) \) and \( V_o(t) \) are corresponding to total applied voltage and the output voltage on the integrating capacitor respectively. If \( R_p \) is large, which means the sample is a perfect insulator, the voltage on \( C_0 \) will show the integrated flowing charge through the ferroelectric sample. The ferroelectric polarization switching current will introduce a phase shift which can be demonstrated in a plot of \( V_o(t) \) vs. \( V_i(t) \). The polarization density can be calculated by

\[ P = \frac{C_0 V_o(t)}{A} \tag{2.3} \]

and the electric field is given by

\[ E = \frac{V_i(t)}{d} \tag{2.4} \]

From equations (2.3) and (2.4), it can be seen that \( P \) and \( E \) are proportional to \( V_o(t) \) and \( V_i(t) \) respectively. The plot of \( V_o(t) \) vs. \( V_i(t) \) actually demonstrates the ferroelectric hysteresis behavior. But several things must be kept in mind that might affect the result.
The equations (2.3) and (2.4) are only approximate. They are accurate only when the following conditions are met. The first condition is that the integrating capacitor $C_0$ is extremely large compared to the linear capacitance of the ferroelectric sample, so that the voltage $V_0(t)$ can be taken as the total voltage drop across the sample. The second condition is that there are no other layers within the sample that will share the electric field with the ferroelectric film. The third condition is that the leakage of the sample is small, as this leakage will introduce another phase shift to mess up the interpretation of the P-E curve. In real experiments the sample's linear capacitance is first obtained from the high-frequency C-V measurement and the right integrating capacitor is chosen according to this value. In the MFS structure the Si substrate will always share a part of the electric field across the whole sample. The real voltage drop across the film is determined also by a C-V measurement, which will be discussed in detail in Chapter 4. The leakage current of the sample is often a big problem and should always be avoided by optimizing the film processing to make well electrical insulating films. If there is still a big leakage, a compensating resistor $R_0$ can be introduced in parallel with the integrating capacitor. The circuit analysis [19] indicates that if $R_0$ is chosen according to equation (2.5)
\[ R_0 = \frac{R_p C_1}{C_0} \]  

(2.5)

then the leakage current can completely flow through the compensating resistor, and equations (2.3) and (2.4) still hold true.

2.3 Experimental setup of Sawyer-Tower circuit

The experimental setup of the Sawyer-Tower circuit is illustrated in Fig. 2.3. The voltage source is a Wavetek 178 waveform synthesizer that can supply a variety of precise waveforms such as sine, square, triangle and pulse. Its bandwidth is 50MHz. Since the maximum output voltage amplitude is only 20V, a transformer with a step-up

![FIGURE 2.3 The experimental setup of Sawyer-Tower circuit](image)
ratio of 1:10 is used to increase the voltage amplitude because the coercive field of the LiNbO₃ is quite large. The sample platform and the probe are placed in an electric/light shield box. The voltage inputs and outputs are monitored with two 10X passive probes whose inputs are 10MΩ and 8pF each. The integrating capacitor is generally larger than 10nF and its leakage resistance is often higher than 30MΩ. Since the sample platform is working on a floating mode, a parasitic capacitance is introduced to the system from the bottom electrode probe tip to the ground. The best way to eliminate this is to connect an operational amplifier to the bottom Au plate to supply a "virtual ground" to it. However, the amplifier will limit the bandwidth of the measurement system, and the integrating voltage signal will be inverted. This means that an additional step is needed for data transforming and increases the data analyzing complexity. By further checking the experimental set-up, it is found that if the outer shield of the probe is properly grounded, the parasitic capacitance will be extremely small compared to the integrating capacitor. As this parasitic capacitance is in parallel with the integrating capacitor, it should not introduce a large error. Comparing these two methods on a given sample demonstrates that there is no observable difference between the two measurement results. Therefore a "virtual ground" is not necessary in our measurement setup.
Chapter 3

Switching Transient Current

3.1 Switching kinetics

When a large enough electric field is applied to the ferroelectric material, all domains with antiparallel directions will begin to reorient their polarization directions. This switching process is generally divided into three stages. The first stage is the nucleation of the new parallel domains at the surface. The nucleation probability depends on the applied field and the surface state. Only when nucleates grow to a critical size can the new domains begin to grow quickly. This nucleation time is about $1\text{ ns}$ and the critical size is about $1-10\text{ nm}$ $^{[2]}$. In second stage the new domains begin to grow across the film. The growth speed is about that of sound; thus the growth time is about $1\text{ ns}$ for a film $1\mu\text{m}$ thick. During the growth period the new domain itself also spreads sideward in the film by a domain wall motion that corresponds to the third stage. This sideway growth time is generally slow compared to the other two switch time constants. It varies from nanosecond to microsecond. The relative values of nucleation time, forward growth time and sideway growth time are quite different in different materials. This leads to the different curve shapes of the switching transient. Theoretical models have been proposed to express the switching time with the three basic parameters above$^{[20,21,22]}$.

The ferroelectric hysteresis loop is important in determining the characteristic parameters such as $P_r$, $P_s$ and $E_c$. But it cannot offer insights into the switching kinetics, since at each point the sample is in its “equilibrium” state. To study the switching mechanism, the microscopic observation of the ferroelectric domain change of its
nucleation, its growth and its domain wall moving, is ideal but is hard to accomplish in the experiment. A switching transient current analysis offers an indirect way of studying the switching kinetics.

3.2 Switching transient

The ferroelectric switching transient current is the polarization current response under a constant electric field. There are two advantages for doing this transient analysis. One is that the dynamic ferroelectric polarization reversal process can be studied by fitting the transient curve to certain theoretical predictions as mentioned above. The other is that this process actually simulates the pulse programming operation for FeNVRAM or MFSFET applications. Thus the necessary operation parameters such as the pulse width and the pulse amplitude can be obtained. Fig. 3.1 illustrates different transient current responses of a ferroelectric film sample. Assuming the pulse rise time is quite fast compared to the switching time constant of the sample, when polarization switching occurs, two peaks are expected to appear in the transient current curve as illustrated in Fig.3.1 (c). The first spike is due to the dielectric response of the ferroelectric material charging. The time constant of this spike depends on the circuit $RC$ time constant. The second peak corresponds to the maximum ferroelectric switching current. The total area under the switching current curve is the sum of the dielectric charge and the switched ferroelectric polarization charge, which is given by

$$\int_0^t i(t)dt = \varepsilon_0 \varepsilon_r EA + (P_m - P_f)A$$  (3.1)
FIGURE 3.1 Different transient curves for a P-S study: (a) applied pulse (b) linear capacitance non-switching current (c) polarization switching current (d) break down current (After Merz [23])
where $\varepsilon_r$ is the relative dielectric constant, $P_M$ is the polarization at the maximum applied voltage and $P_r$ is the remnant polarization density. The switching time $t_s$ is usually taken as the value when the switching current amplitude falls to $0.1i_{\text{max}}$, because it is hard to precisely measure the total switching time. The first term of equation (3.1) is the linear charging current and the second term is the polarization switching current. If there is no switching current and the sample has not broken down, only the first spike can be observed, as in Fig. 3.1 (b). While if the sample breaks down, the sample acts as a short circuit and the current has the same shape as the applied pulse, as in Fig. 3.1 (d).

The exponential behavior of switching transient currents has been reported and studied extensively\textsuperscript{[24,25,26]}. These curves are often fitted with Avrami-Ishibashi model\textsuperscript{[27]}. This model gives the expression of switching time as

$$t_s = t_\alpha e^{-a/E}$$

(3.2)

In this equation $\alpha$ is called the activation field. It is much higher than the coercive field. At very high fields, this relation changes to a power law in the form of $t \sim E^n$, where $n$ depends on the material. The maximum switching current can be described by

$$i_{\text{max}} = i_\alpha e^{-a/E}$$

(3.3)

Constants $\alpha$, $n$, $i_\alpha$ and $t_\alpha$ are all temperature dependent, with the switching time decreasing as the Curie point is approached.
3.3 Circuit for measuring transient current

3.3.1 Circuit analysis

The schematic circuit for measuring the polarization-switching transient is shown in Fig. 3.2.

![Circuit Diagram]

**FIGURE 3.2** Circuit for measuring the polarization switching transient current

The idea of this circuit is quite straightforward. The pulser generates a fast rise pulse. This pulse is delivered to the ferroelectric sample that is in series with a resistor R3. If the pulse amplitude is sufficiently high to switch the sample, the switching current as illustrated in Fig. 3.1 (c) should be observed through the voltage drop on R3.

However, several considerations should be taken into account. The first is how to deliver the fast rise pulse to the sample. A pulse is actually the sum of a series number of harmonic sine waves. To achieve an exact replica of a pulse with a very fast rise time, infinite harmonics are ideal. This means that the pulse transfer is within the high-frequency application range. When the electromagnetic wave has a high frequency, the
voltage and the current no longer remain spatially uniform compared to the geometric size of the discrete circuit elements. They have to be treated as propagating waves. Since Kirchhoff’s voltage and current laws do not account for these spatial variations, the traditional lumped circuit analysis should be modified. A transmission line theory is thus developed for this reason. In this theory, the wire itself plays an important role in circuit designing and is called a transmission line \(^{28}\). The transmission line is treated as a distributed circuit and analyzed with the combination of Kirchhoff’s laws and electromagnetic theory. The result of this analysis is the definition of a characteristic impedance of the transmission line system. For each transmission line system, the end load should be properly terminated so that no reflection wave exists and the desired power can be properly transferred to its destination. In Fig. 3.2, R1 and R2 are two terminating resistors that have the same characteristic resistance as the transmission line. Strictly speaking, at the R2 end the terminating impedance is not exactly equal to the transmission line characteristic impedance because R2 is in parallel with the series combination of the sample and R3. However, in our measurement the samples generally have very small capacitances, therefore their impedances are quite large compared to R2. The terminating impedance approximates to R2 quite well.

The second consideration is the sample charging time. As the sample is actually a capacitor, the charging time constant RC should be small enough so that it cannot be misidentified as the switching time. For this reason, a small capacitance is desired. That is why spots with small electrodes are preferred. There is also another reason in favor of small capacitances. Though different researchers have presented different reports on how
the electrode area affects the switching time\textsuperscript{[29,30]}, one generally accepted conclusion is that ferroelectric capacitors with small electrode areas should have a shorter switching time.

As a third consideration, changing the applied pulses input waveform could make further improvement. A dual-polarity four-pulse chain is used for investigating the transient behavior. This is illustrated in Fig. 3.3.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure3.3.png}
\caption{(a) Dual-polarity four-pulse chain (b) Full stable switching transient (c) Unstable switching transient}
\end{figure}
The advantage of this pulse chain is that it offers a great variety of pulse parameter selections so that it is quite flexible to study the switching behavior. Fig. 3.3(a) is the four-pulse chain. The positive and negative polarity pulses can be adjusted separately. For two consecutive positive/negative pulses, the pulse amplitude, pulse width (PW+/PW-) and distance between two leading edges are all variable parameters. The time interval between positive pulses and negative pulses is also adjustable. If the first pulse can fully switch the antiparallel domains, a transient current with the shape in Fig. 3.1. (c) can be observed. Assuming the domains cannot switch back, i.e., assuming a stable switching, only discharging current will appear when pulse is zero. When the second pulse rises, as there are no switchable domains, only charging current is observed. Then the capacitor discharges again. When the first negative pulse is applied those switched domains will be restored to their original direction, so the “bell” shape current appears for a second time. The following responding curves are similar as the corresponding ones in positive pulse chain except that the polarity is inversed. During the first positive pulse, the switched polarization charge can be calculated by using equation (3.1) except $P_r$ is replaced by $P_r$. The negative sign in subscript means $P_M$ and $P_r$ have different directions. In the second pulse a positive sign for $P_r$ is used to show that $P_M$ and $P_r$ have same direction and the calculated charge is the unswitched charge. By subtracting these two charges, the total charge of $P_{r+}-P_r$ is obtained.

In real materials, all kinds of curves can be recorded. Fig. 3.3. (c) shows such an example which was reported by Rost.\textsuperscript{[31]} If in the first positive pulse the antiparallel domains are switched, a full switching transient current still can be observed. But if this
switching is unstable, the switched domains may switch back immediately after the pulse. So not only the discharging current, but also the back switching current appears when the pulse is zero. The same current will come out in the second positive pulse, and it is obvious that no switching current will come out in negative pulses. This phenomenon is called imprint, which means ferroelectric film has a preferred polarization direction. The reason for this may due to the non-uniform distribution of defects within the film.

3.3.2 Experimental setup

The experimental setup for the switching transient current measurement circuit is shown in Fig. 3.4.

**FIGURE 3.4** The experimental setup for measuring the switching transient with a dual-polarity four-pulse chain pulse generator
The pulse generator is an Avtech AVR-3-PS-PN-Ru3 that can produce the dual-polarity four-pulse chain. The pulse width range can be adjusted from 100ns to 1ms, and the maximum output voltage amplitude is 150V to a high load impedance. This pulse generator is triggered with a Stanford pulse generator that is capable of both single burst and repetitive trigger. The designed output resistance of the pulse generator is 0Ω, so a 50Ω resistor is put in series at the output of it for termination, because in this set-up all wirings are RG-58U coaxial cables with characteristic impedance of 50Ω. To transfer the pulse chain to the sample as smoothly as possible, the terminating resistor at the sample end should be put as close as possible to the sample. This is done by putting a 50Ω chip resistor inside the body of the probe. The transient current is monitored through another 50Ω resistor, which also acts as a terminator at the input of the oscilloscope. The oscilloscope is a state-of-the-art TDS 3054 four-channels color digital phosphor oscilloscope with bandwidth of 500MHz and sampling rate of 5Gs/s. The fastest rise time this scope can measure is \[^{[32]}\]

\[
\tau_r = \frac{0.35}{BW} = 0.7\,ns
\]  

(3.4)

which is quite small compared to the rise time of the generated pulse. All data are digitized and transferred to a computer. The oscilloscope is also triggered with the Stanford pulse generator to synchronize the pulse generator and the oscilloscope.
Chapter 4

Capacitance vs. Voltage Bias Hysteresis

4.1 Capacitance vs. voltage (C-V) measurement

4.1.1 Theory of C-V hysteresis

The capacitance vs. voltage (C-V) measurement has been a standard characterization method in the semiconductor industry. Sze gives a very good summary in his book [33]. A typical C-V curve on p-Si substrate of a Metal-Insulator-Semiconductor (MIS) structure is shown as Fig. 4.1. For a n-type substrate, the curve shape is basically the same except that it needs to be flipped.

![Diagram of C-V curve](image)

**FIGURE 4.1 The C-V curve of a Metal-Insulator-Semiconductor structure on a p-Si substrate**
As the MIS structure can be treated as the series combination of the insulator capacitance and the substrate capacitance, a measurement of the capacitance vs. applied voltage can demonstrate the transition from the accumulation to depletion and then to inversion in the MIS structure. The solid line in Fig. 4.1 is the static C-V curve which is measured under a small frequency. If the measurement signal changes so fast that the minority carriers recombination-generation rate cannot keep up with it, the high-frequency C-V curve does not show a capacitance increase in the inversion region.

In the above discussion only the insulator thickness and its dielectric constant are considered for an ideal metal insulator capacitor structure analysis. This is certainly not true in the real world, as there are all kinds of parasitic effects that need to be included in analyzing a C-V curve. For a practical diode, interface traps and oxide charges exist within the insulator film and affect greatly the MIS characteristics. A basic classifications of these traps and charges is: (1) interface trapped charges $Q_{it}$, which are produced by the excess silicon and excess oxygen and impurities; (2) fixed oxide charges $Q_{fr}$; (3) oxide trapped charges which can be created by x-ray radiation and hot-electron injection; (4) mobile ionic charges $Q_m$, such as sodium ions. The net effect of all these charges can be equivalently expressed as a thin layer charges $Q_o$ at the semiconductor and insulator interface. The C-V curve will thus shift according to
\[ \Delta V = \frac{Q_0}{C_i} \]  

(4.1)

In the semiconductor industry, the charges discussed above are always carefully avoided as they often deteriorate the device performance. But for a MFSFET application, ferroelectric charges are deliberately controlled near the semiconductor surface to adjust the channel current. A high-frequency C-V hysteresis can then be observed as in Fig.4.2. When the measurement starts from the negative bias, negative polarization charges will be at the ferroelectric film-semiconductor interface. As this is a p-type semiconductor substrate, holes will be attracted and accumulate on the semiconductor surface. Compared to a non-polarization condition, this will make it more difficult for the external bias to deplete the semiconductor, so the flat-band voltage shifts toward the positive bias direction. When the external positive bias is strong enough to switch the polarization direction, positive charges will exist at the interface, and when the bias sweeps back these charges will repulse the holes in semiconductor and make it more difficult for them to accumulate. For this reason a clock-wise rotation C-V hysteresis can be observed. The same analysis also applies for an n-type substrate structure, and the resulting hysteresis curve has a counter-clockwise rotation. The hysteresis window size, i.e., the difference between the flat-band voltages, is proportional to the coercive field \(^{[10]}\).
FIGURE 4.2 The theoretical p-type C-V hysteresis curve compared to classic MIS C-V curve

4.1.2 Charge injection and surface potential

One of the most important applications of this C-V measurement is to determine whether the hysteresis behavior is caused by the desired polarization charges or by the injected charges from the semiconductor. In ferroelectric memory device processing, the high interface trap density often introduces charges injection from the semiconductor into the film. These injected charges will also lead to a hysteresis curve, but the rotation direction of the hysteresis curve is opposite to that caused by polarization charges. The polarization charges and injected charges may often exist at the same time and compete with each other. According to Fleetwood et. al.\textsuperscript{[34]}, the existence of the charge injection
can be found by reducing the bias sweeping rate, because the communicating time of
the injected charge with the underling substrate is longer than that of the polarization
charge. So the injection charge effect is more noticeable at lower sweep rates. The shrink
of the hysteresis window, or even the reverse of the rotation direction, will demonstrate
the existence of the charge injection\textsuperscript{[35]}. The C-V curve thus offers a convenient way to
study the charge injection effect.

Another useful aspect of the C-V measurement is the determination the surface
potential. This is quite important for MFS structure characterization, because the surface
potential varies with the applied bias. The real voltage applied on the ferroelectric thin
film differs from the applied external bias. In analyzing the switching behavior, the true
electric field across the film must be known. So the potential drop on the semiconductor
substrate should be measured. The surface potential is given by

\[
\Psi_s(V) = \int_{V_{flat}}^{V} \left[1 - \frac{C}{C_i}\right] dV
\]

(4.2)

where $\Psi_s(V)$ is the surface potential or the potential drop on the semiconductor
substrate, $V_{flat}$ is the flat-band voltage, $C$ is the measured capacitance corresponding to $V$
and $C_i$ is the film capacitance. Since in the accumulation region only the film itself stores
charge, so the measured capacitance $C_{acc}$ is actually equal to $C_i$. The flat-band voltage is
the voltage where depletion region begins, which can also be read from the C-V curve. The voltage across the film can thus be calculated by subtracting $\Psi_s(V)$ from the total applied voltage, and the electric field obtains by dividing it with the film thickness.

4.2 Experimental setup

The C-V measurement is accomplished with a HP 4284A precision LCR meter. This equipment is capable of doing measurements in the range of 20Hz~1MHz. The internal oscillator voltage level range is 5mV~20Vrms and current level is within 50μA~200mArms(option 001). The DC bias level is 0~40V, and the maximum DC bias current can reach 100mA \cite{36}. To reduce the interference, the output terminal of the 4284A takes a four-terminal pair configuration in Fig. 4.3(a). With this set-up, the outer shield conductor acts as the return path of the measurement signal current. The same current thus will flow through the center conductor and the outer shield in opposite directions so that the magnetic fields generated by this current will cancel each other. The self/mutual inductance can be eliminated in this way. Since the test leads extension is necessary due to the physical setup limitation of the sample platform, the four-terminal extension wires are connected into a shielded two-terminal setup at the platform end, as shown in Fig. 4.3(b). This has the advantage of reducing the inductance pick up.
(a)

FIGURE 4.3 (a) Four-terminals pair configuration of HP4284A input terminal and (b) two-terminal extension (HP 4284A LCR meter manual, 1988)
Chapter 5

Leakage Current Analysis

5.1 Introduction

When ferroelectric films are integrated into memory cells, they must always have good electric insulation properties. This is obvious for DRAM applications because information can be stored safely with longer refresh time. It is also important to understand the nature of the leakage current for FeNVRAM and MFSFET, in order to control heating of the memory to avoid thermal breakdown. In general, most ferroelectric materials are very good insulators. The LiNbO₃ bulk crystal has a resistivity of $10^{18} \Omega \cdot \text{cm}$. However, in practice, ferroelectric films are not as perfect insulators as they are in bulk. Due to structural imperfections such as vacancies, mobile ions, grain boundaries and film electrode interface traps, a relatively high density of charge carriers may exist and flow through the film under an external bias. The conducting mechanisms of these holes, electrons and ions are rather complicated and they are often present at the same time. Unfortunately, they are not simply additive, and the leakage current indeed often demonstrates a rather irregular nonlinear behavior. The identification of the dominant transport mechanism is the key to understanding the relationships of the film property to the resulting current-voltage characteristics. This knowledge of the dominant conduction mechanism can be used to reduce the leakage current level.
5.2 Conduction mechanisms

There is a rich array of electrical conduction mechanisms. They can be divided into two broad categories: barrier-limited and bulk-limited.

5.2.1 Barrier-limited

a. Schottky Emission

This mechanism is operative in the vicinity of the contact and the insulator interface. The detailed theory has been discussed in many textbooks on semiconductor devices \cite{33,37}. When two materials with different work functions are placed in contact with each other, e.g., a metal and a ferroelectric film, the mismatch of the work function will lead to a barrier formed on the interface. The barrier height depends on the difference between the metal work function and the electron affinity of the ferroelectric.

\[
\phi_{B0} = \phi_m - \chi
\]  

(5.1)

Equation (5.1) gives the barrier height where \( \phi_m \) is the metal work function and \( \chi \) is the electron affinity of the ferroelectric film material. When an electric field is applied, a Schottky effect \cite{33} will exist to lower the barrier height by the amount as in equation (5.2).

\[
\Delta \phi = \frac{eE}{\sqrt{4\pi \varepsilon_d}}
\]  

(5.2)
This is illustrated in Fig. 5.1 for a vacuum case, and is due to the attractive force between the electrons injected from the cathode into the ferroelectric film and the "image" positive charge in the cathode when an electric field is applied. The quantity $\varepsilon_d$ is not the static permittivity because the transit time of the electrons moving through the barrier is quite short compared to the dielectric relaxation time. The ferroelectric does not have enough time to be polarized, so $\varepsilon_d$ is actually $\varepsilon_m$, which is smaller than $\varepsilon_{DC}$. The quantity "$E$" is the maximum field in the junction region. It should be larger than the average field $V/d$. For PZT, BST and SBT films $\Delta \phi$ is about $0.8eV_{[2]}$. This correction is large since it is almost half of $\phi_B$ itself. The Schottky barrier can be greatly reduced and

![Diagram](image)

FIGURE 5.1 The Schottky effect between a metal surface and the vacuum (After Sze$^{[13]}$)
lead to a larger leakage current. The current density equation is given as \(^{33}\)

\[
J = A^* T^2 \exp \left[ \frac{-e(\phi_{b0} - \sqrt{eE/4\pi\varepsilon_d})}{kT} \right]
\]  \hspace{1cm} (5.3)

in which \(A^*\) is the effective Richardson constant, \(T\) is the temperature, and the term in the parentheses corresponds to the effective barrier height discussed above.

b. Tunneling

Schottky emission current often dominates at low electric fields. When the depletion width of the ferroelectric film is small and the applied electric field is large, Fowler-Nordheim currents (quantum mechanical tunneling) begin to take effect. When the depletion width is reduced as to be comparable to the electron wavelength, there is a probability that electrons can exist in the film. This means that electrons from the electrode can penetrate horizontally into the conduction band states of the film rather than jump over the barrier \(\phi_{b0}\) vertically. The tunneling current is given by

\[
J \sim E^2 \exp \left[ -\frac{4\sqrt{2m^*}(e\phi_{b0})^{3/2}}{3\varepsilon_0hE} \right] \]  \hspace{1cm} (5.4)

and \(m^*\) is effective mass. The tunnel emission has a very strong dependence on the applied voltage but is essentially independent of temperature.
5.2.2 Bulk-limited

a. Ionic conduction

The ionic conduction mechanism has been well studied. It is similar to a diffusion process illustrated in Fig. 5.2 (b). Ions can hop from one position to another available position, either a vacancy or an interstitial site in the crystal lattice. The energy required to surmount the energy barrier comes from thermal energy fluctuations. So it is highly temperature dependent. In semiconductor devices, the ionic conduction is mainly due to the impurity ions, not to the intrinsic ions. These ions are small mobile ions such as sodium or lithium ions, which come from the starting material or from the processing. Generally the DC ionic conductivity decreases during the time when the electric field is applied, because these ions cannot be easily extracted from the insulator. So they will build up when they migrate to the metal-insulator or insulator-semiconductor interface under the applied electric field, causing a distortion of the potential distribution. This has been a severe problem in MOSFET fabrication. The ionic current density is given by

\[ J \sim \frac{E}{T} \exp(-\Delta E_{at} / kT) \]  \hspace{1cm} (5.5)

where \( \Delta E_{at} \) is the activation energy of the ions. The ionic conduction can be avoided by extreme care in clean room controlling, or using \( P^+ \) or \( Cl^- \) ions to bind up and neutralize the mobile positive ions of \( Na^+ \) or \( Li^+ \).
b. Ohmic conduction

The theory of the ohmic conduction can be found in most of the solid-state physics textbooks \[^{[38]}\] and is well understood. The basic idea is that the electrons don’t have a continuous energy distribution, but are distributed in energy bands in which some energy levels are forbidden because of the crystal lattice periodicity. The energy difference between the conduction and valence band, the band gap, determines whether the material is a conductor, a semiconductor or an insulator. Only those holes in the valence band and electrons in a not fully filled conduction band can take part in the electric conduction. The mobility of the electrons and holes is affected by the scattering of phonons, impurities and defects. The expression for ohmic conduction is

\[
J \sim E \exp(-\Delta E_{ae} / kT)
\]  
(5.6)

where \(\Delta E_{ae}\) is the activation energy of electrons. Ferroelectric materials generally have a large band gap and a very small ohmic conductivity in the bulk.

c. Frenkel-Poole emission

In real insulator materials, impurities and defects can always exist which have allowed energy states within the band gap. These additional states are called “traps”. The traps can hold either a positive or a negative charge. Under an applied field the potential well distorts asymmetrically, as shown in Fig. 5.2 (c). Trapped charges can escape the well by thermal activation.
FIGURE 5.2 Bulk controlled conduction mechanisms of: (a) space charge limited (b) Ionic and (c) Frenkel-Poole emission \[39\]

This process is quite similar to that of the Shottky barrier conduction. The current density is given by

\[ J \sim E \exp\left[-\frac{e(\phi_m - \sqrt{eE/\pi\varepsilon_d})}{kT}\right] \]  

(5.7)
and $\phi_m$ is the barrier height of the trap. Qualitatively the Frenkel-Poole effect can be separated from the Shottky effect by making the top and the bottom electrodes of different materials, and by measuring the leakage currents with positive and negative polarity. Frenkel-Poole emission should have a symmetric leakage current behavior under these asymmetric conditions.

d. Space Charge Limited Currents (SCLC)

When all conduction mechanisms discussed above reach a certain threshold, the already injected charges into the films will have a major limit on the leakage current, as in Fig. 5.2(a). This is because at this time the rate of charge injection will exceed the rate at which the charges transported through the film. These charges fill the space between the cathode and the anode, so they are called “space charges”. The space charges will discourage further charge injection. If traps are present in the film, the SCLC will be reduced, because empty traps remove carriers. In this regime, the leakage current is given by

$$J = \frac{8\varepsilon_0 \mu V^2}{9d^3}$$

(5.8)

which is known as the Mott-Gurney law. For ferroelectrics, some modifications are made to equation (5.8)\textsuperscript{[2]}. The film thickness $d$ is more accurately given by $d-2a'$, where $a'$ is an
accommodation or mutual diffusion length near the electrode. There is also a temperature correction, which gives

$$J(V,T) = \text{constant} \frac{V}{d} \left( \frac{V}{d^2} \right)^{T^*/T} \tag{5.9}$$

and $T^*$ is related to the trap states density per unit energy near the Fermi surface of the ferroelectric, and in general it is approximately equal to room temperature. A summary of all the conduction mechanisms is given in Table 5-1.

5.3 Experimental setup

The I-V measurement is accomplished with a HP 4140B pA meter/DC voltage source. To realize stable low-current measurements from $10^{-9}$A down to $10^{-12}$A, care has been taken in the wiring to minimize the external noise. The connection of the measurement setup is illustrated in Fig. 5.3(a), and the wiring is illustrated in Fig. 5.3(b). The interference noise is reduced by employing a low-guard method, where the "LOW" terminal (the inner braid of the current input connector) of the pA meter is grounded. The whole setup is put in an electric/light-shielded box. The measurement signal is converted to a digital signal and then collected in a computer through the HPIB interface.
### Table 5.1 Conduction mechanisms in insulators

<table>
<thead>
<tr>
<th>Mechanism</th>
<th>Expression</th>
<th>Voltage and temperature dependence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schottky emission</td>
<td>$J = A^* T^2 \exp \left[ -e(\phi_{bo} - \sqrt{eE / 4\pi\varepsilon_d}) / kT \right]$</td>
<td>$\ln J / T^2 \sim \sqrt{V / T}$</td>
</tr>
<tr>
<td>Tunneling</td>
<td>$J \sim E^2 \exp \left[ -\frac{4\sqrt{2m^* (e\phi_{bo})^{3/2}}}{3e\hbar E} \right]$</td>
<td>$\ln J / V^2 \sim 1 / V$</td>
</tr>
<tr>
<td>Ionic</td>
<td>$J \sim \frac{E}{T} \exp (-\Delta E_{ad} / kT)$</td>
<td>$J \sim \frac{V}{T} \exp (-\text{const} / T)$</td>
</tr>
<tr>
<td>Ohmic</td>
<td>$J \sim E \exp (-\Delta E_{ad} / kT)$</td>
<td>$J \sim V \exp (-\text{const} / T)$</td>
</tr>
<tr>
<td>Frenkel-Poole emission</td>
<td>$J \sim E \exp \left[ -e(\phi_{bi} - \sqrt{eE / \pi\varepsilon_d}) / kT \right]$</td>
<td>$\ln J / V \sim \sqrt{V} \beta^* / kT$</td>
</tr>
<tr>
<td>Space Charge Limited</td>
<td>$J = \frac{8\varepsilon_d \mu V^2}{9d^3}$</td>
<td>$\sqrt{J} \sim V$</td>
</tr>
</tbody>
</table>

* $\beta^* = e \sqrt{\frac{e}{\pi\varepsilon_dd}}$
FIGURE 5.3 The experimental setup of I-V measurement: (a) connection and (b) wiring (HP 4140B manual)
Chapter 6

Experiment Results

6.1 Sample structure and XRD analysis

The sample used for characterization has the structure as illustrated in Fig. 6.1. The top electrodes are Au dots that are deposited through an Al mask. Big dot has an area of 0.00378cm$^2$ and small dot has an area of 0.00189cm$^2$. The bottom electrode is a p-type Si(111) substrate. For correct electrical characterization results, the bottom of the sample should have a good ohmic contact with the measurement platform. This is accomplished by making an Al layer at the bottom of the Si substrate through DC sputtering $^{[40]}$. The sample is then attached tightly on the platform by the mechanical pump.

![Diagram of the Metal-Ferroelectric-Semiconductor structure]

**FIGURE 6.1 The Metal-Ferroelectric-Semiconductor structure**
The samples are made with RF sputtering by using the parameters optimized by Rost \cite{31}. X-ray diffraction (XRD) analysis is used to determine the sample composition and structure. The XRD pattern is given in Fig. 6.2.

![XRD pattern](image)

**FIGURE 6.2** The XRD pattern of the RF sputtering grown sample with a (006) preferred orientation

Two strong peaks are observed in the XRD pattern, which correspond to Si(111) and LiNbO$_3$ (006). Since in the LiNbO$_3$ powder pattern the amplitude of the (006) peak is only about 4\% of the strongest peak (012), this XRD demonstrates that the sample is highly oriented.

The thickness of the sample is measured with an ellipsometer. The incident laser wavelength is 6328Å and incident angle is 70°. The thickness is determined to be 0.34μm and the refractive index is measured to be 2.3. The color of the thin film matches the
color chart of LiNbO$_3$ on the Si substrate, which verifies the ellipsometer result from another point of view.

6.2 P-E Hysteresis Curve of LiNbO$_3$ MFS capacitor

The MFS capacitor parameters R$_p$ and C$_p$ are obtained from C-V and I-V measurements. C$_p$ is read from C$_{acc}$ in Fig. 6.6(a) and is about 540pF. So the impedance of the selected 18 nF integrating capacitor is small enough compared to the impedance of C$_p$ when the applied sine wave frequency is 1KHz. The I-V curve is not linear when the applied voltage is increased. But within a 10V range as in Fig. 6.7, the amplitude of the DC leakage current is still quite small compared to the integrating current, so no compensating resistor is required. A series of V$_{o}(t)$ vs. V$_i(t)$ curves are shown in Fig. 6.3(a). The input waveform is a 1KHz sinusoidal wave and the maximum applied voltage amplitude is about 50V. The values of P$_r$ and E$_{cr}$, which are listed in table 6.1, increase with higher applied voltage. The applied voltage amplitude cannot go higher than 60V, because the sample electrode ablates at this electric field, which is about 1.75MV/cm. When the electrode ablates, an open circuit is formed under the test probe, so that no further electric field can be applied on the sample. This is not caused by the dielectric break-down, since moving the probe to another spot on the same electrode allows one to repeat the previous experiment. In the case of dielectric breakdown, the sample will be
completely destroyed and the experimental results could no longer be repeated at all on the same sample.

### TABLE 6.1 Values of $P_r$ and $E_c$ at various applied electric fields

<table>
<thead>
<tr>
<th>Max Applied field (KV/cm)</th>
<th>$P_{r+}$ ($\mu$C/cm$^2$)</th>
<th>$P_{r-}$ ($\mu$C/cm$^2$)</th>
<th>$E_{c+}$ (KV/cm)</th>
<th>$E_{c-}$ (KV/cm)</th>
<th>Avg$P_r$ ($\mu$C/cm$^2$)</th>
<th>Avg$E_c$ (KV/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>125.3</td>
<td>6</td>
<td>-13.8</td>
<td>90.4</td>
<td>-47.2</td>
<td>9.9</td>
<td>68.8</td>
</tr>
<tr>
<td>286.2</td>
<td>13.3</td>
<td>-20.4</td>
<td>137.1</td>
<td>-97.4</td>
<td>16.85</td>
<td>117.25</td>
</tr>
<tr>
<td>452.7</td>
<td>15.4</td>
<td>-24.6</td>
<td>161.2</td>
<td>-101.7</td>
<td>20</td>
<td>131.45</td>
</tr>
<tr>
<td>616.5</td>
<td>19</td>
<td>-27.9</td>
<td>184.8</td>
<td>-122.3</td>
<td>23.45</td>
<td>153.55</td>
</tr>
<tr>
<td>780.9</td>
<td>22.3</td>
<td>-30.3</td>
<td>201.6</td>
<td>-143.9</td>
<td>26.3</td>
<td>172.75</td>
</tr>
<tr>
<td>1140</td>
<td>25.9</td>
<td>-34.8</td>
<td>231.7</td>
<td>-163.1</td>
<td>30.35</td>
<td>197.4</td>
</tr>
<tr>
<td>1340.9</td>
<td>28.2</td>
<td>-35.4</td>
<td>235.5</td>
<td>-189.2</td>
<td>31.8</td>
<td>212.35</td>
</tr>
<tr>
<td>1539.7</td>
<td>29.6</td>
<td>-37.1</td>
<td>251.6</td>
<td>-197.6</td>
<td>33.35</td>
<td>224.6</td>
</tr>
</tbody>
</table>

When transferring from the curve (a) to the curve (b), the maximum surface potential is determined from equation (4.2) by Fig. 6.4(a), which is about 0.59V. This does not change the voltage applied on the ferroelectric film too much. Fig. 6.3 (b) is a $P$-$E$ curve with $P_r=16.85\mu$C/cm$^2$ and $E_c=117.25$ KV/cm, when the maximum applied field is 286.2KV/cm.
FIGURE 6.3 (a) Series curves of integrating voltage vs. applied voltage and (b) polarization vs. electric field curve with applied voltage of 10V
6.3 Switching transient current

The switching transient current is measured with the dual-polarity four-pulse chain. As a switching time of 500ns has been reported \cite{11} for LiNbO$_3$, the applied pulse width is chosen to be 800ns. The rise time of the applied pulse is about 10ns and the fall time is about 110ns. Both the applied pulses and the resulting transient curves are shown in Fig. 6.4(a), for an applied pulse amplitude of 20V. The first transient from Fig. 6.4(a) is enlarged in Fig. 6.4(b). The first transient for a 60V pulse amplitude is also given in Fig. 6.4(c). The insert plot in Fig. 6.4(b) is the linear discharging current for a 250mV pulse amplitude. Only one peak appears and the decaying time is 41ns that matches well with the calculated 3RC decay time of 40.5ns. This demonstrates that no polarization switching occurs under this electric field. When the applied pulse amplitude increases, two peaks are found in the transient current curve as shown in Fig. 6.4(b) and (c), which corresponds to the ferroelectric switching current. The switching time under a 20V amplitude is 97ns, and when the amplitude increases to 60V the switching time reduces to 88ns. However, the retention is very short, so when the pulse is zero, another peak is shown corresponding to a back-switching polarization current. This phenomenon might be due to the depolarization field inside the film in this MFS structure. Because the semiconductor electrode has a longer screening length than a metal electrode, the polarization charges cannot be completely compensated and an internal large depolarization field might build up.
FIGURE 6.4 (a) The switching transient current under four-pulse chain for a pulse amplitude of 20V, (b) enlarged transient current plot of (a) in first pulse, (c) switching current under 60V
FIGURE 6.5 P-E hysteresis loops corresponding to continuous sine wave and discrete pulses

Fig. 6.5 gives a qualitative explanation of the difference between a continuous P-E measurement and a discrete pulse measurement. Before the external bias is applied, the original stable polarization state will show a 0 net polarization for a polycrystalline film. When a continuous wave such as the sine wave is applied on the sample, the polarization charges will respond as the curve 0 in Fig. 6.5. If the external drive voltage is a pulse, the polarization will first respond as curve 1 and then drops as curve 2 since it has a fast falling edge. Since a time interval of 0 bias is allowed between two consecutive pulses, enough time is available for switched polarization charges to relax back to their original directions due to the depolarization. The same curve will repeat for the second pulse with the same polarity. If the polarity is reversed the corresponding curves are 3 and 4.
6.4 C-V measurement

The C-V hysteresis with a clockwise rotation hysteresis loop is illustrated in Fig. 6.6(a). The whole curve is not symmetric about 0, but has a shift to the positive direction. This agrees with what has been observed from the P-E measurement. The hysteresis window, defined as the difference between the two threshold voltages, is about 1.6V. The surface potential of the substrate is calculated from equation (4.2). The maximum potential drop begins when a strong inversion starts. The surface potential is about 0.59V and it corresponds well to the value calculated from a substrate doping level of 0.575V. When the electric field increases, the inversion layer screens the further penetration of the applied electric field into the semiconductor substrate. So the surface potential does not increase much since the surface band cannot bend any further.

The rotation direction of the curve corresponds to the hysteresis behavior controlled by ferroelectric charges. To further exclude the existence of hysteresis controlled by the injection charges, C-V curves are measured under sweeping rates of 2V/s, 0.2V/s, 40mV/s and 10mV/s as in Fig. 6.6(b). The rotation direction doesn’t change and no obvious window reduction is founded. This demonstrates that the charge injection is not the dominant mechanism in controlling the C-V hysteresis behavior.
FIGURE 6.6 (a) C-V hysteresis curve and (b) multi C-V curves for different sweep rates
6.5 Leakage current analysis

The I-V curve is illustrated in Fig. 6.7. The conduction behavior is not symmetric, which comes from the asymmetric nature of the MFS structure. As have been discussed in Chapter 5, different conduction mechanism can exist at the same time. However, since different conduction mechanisms may begin to dominate at different electric fields and different temperatures, it is quite possible that within the electric field range of our concern, a dominant conduction mechanism may determine the leakage current level. Therefore, the experimental curve is fitted with different conduction theories discussed in Chapter 5 to check if there is one dominant conduction mechanism existing.

![FIGURE 6.7 The current vs. voltage curve](image)

There are three different zones as illustrated in Fig. 6.7. Zone III and I have nonlinear conduction behaviors and zone II has a linear curve. In zone II the sample
resistance is $1.39 \times 10^8 \Omega$. Since our major concern is how to control the maximum leakage current of the sample. The conduction mechanism in Zone I and III will be discussed in more detail because the leakage current increases greatly within these regions. All the discussions in the following paragraphs are for zone I and III only.

The ohmic and ionic conductions are linear functions of the electric field, so these two effects can be neglected in zone I and III first. As has been discussed, if the Frenkel-Pool emission is dominant, the conduction behavior will be symmetric even though the top and the bottom electrodes are not the same. As is shown in Fig. 6.7, this curve is not symmetrical in the positive and the negative bias regions. This implies that Frenkel-Pool emission is not dominant within these two regions. According to the J-V relation of Frenkel-Pool emission summarized in Table 5-1, the $\text{LnJ}/V - \sqrt{V}$ curves are also studied and illustrated in Fig. 6.8. Though the curve in zone I looks linear, the experimental curve slope is smaller than the slope value that is calculated from the theory prediction of $\frac{\beta}{kT}$ discussed in Chapter 5 by a factor of 3. The curve in zone III is non-linear. Therefore, Frenkel-Pool emission conduction is not dominant within these regions.

The tunneling current may occur at very high electric fields. For our sample, within the measured electric field it is not likely that this tunneling will happen. By fitting the experimental data with the theoretical prediction, the $\text{LnJ}/V^2$ vs. $1/V$ curves shown in Fig. 6.9 give a non-linear curve. This demonstrates that tunneling is not dominant within the measured electric field range.
FIGURE 6.8 Experimental data plotted in $\ln(J/V)$ vs. $\sqrt{V}$ curves for both zone I and III

FIGURE 6.9 Experimental data plotted in $\ln(J/V^2)$ vs. $1/V$ curves for both zone I and III

In zone III, the $\sqrt{J}$ and $V$ curve doesn’t have a linear relation as predicted in Table 5-1 for the space charge limited conduction. This only leaves the possibility of
Schottky emission conduction in zone III. As summarized in Table 5-1, the Schottky emission conduction has a \( \ln(J) \sim \sqrt{V} \) relation. The linear fit of this relation in zone III is illustrated in Fig. 6.10. The slope of the curve is 3.62. It should be equal to 
\[
\frac{e}{kT} \sqrt{\frac{e}{4\pi \varepsilon_0 d}}.
\]
According to this expression, \( \varepsilon_r \) is calculated to be 5.32. Since it should be the optical dielectric constant, then the refractive index \( n \) can be concluded from the square root of it, which is 2.31. This matches with the directly measured value of 2.30 from the ellipsometry measurement quite well. Therefore, in zone III it is the Schottky barrier that mainly controls the leakage current behavior.

**FIGURE 6.10** Experiment and linear fit \( \ln(J) \) vs. \( \sqrt{V} \) curves in positive bias region

In the negative bias region, both the \( \sqrt{J} \) vs. \( V \) curve and the \( \ln(J) \) vs. \( \sqrt{V} \) curve show a good linear fit with the experimental results as illustrated in Fig. 6.11.
According to the discussions of Chapter 5, space charge limited conduction becomes dominant only when enough carriers have been injected into the film and accumulated. Therefore in Fig. 6.9 (b), the linear fit starts not from 0 but from \(-3V\) to allow enough carriers to be injected into the film. Though the linear fit is quite good within this region, the slope of the curve is much too small compared to the theoretical prediction of \(\frac{8e_d\mu}{9d^3}\). This demonstrates that within this voltage range space-charge-limited conduction has not started to make a significant difference.

The Schottky barrier conduction mechanism fits the experimental results in the whole negative bias region. Its slope of 2.3 is a bit smaller than that in the positive bias region of 3.6. This might come from the surface states at the interface between the ferroelectric film and the metal electrode. The leakage current is larger in the positive bias region than in the negative bias regions. This can be explained with a back-to-back Schottky barrier model that will be discussed qualitatively in the following paragraphs.
FIGURE 6.11 Experiment and linear fit curves in negative bias region of: (a) Schottky barrier $\ln(J)$ vs. $\sqrt{V}$ fit and (b) SCLC $\sqrt{J}$ vs. $V$ fit
The band structure of the metal electrode, the LiNbO$_3$ film and the p-Si substrate before they come into contact with each other can be illustrated as Fig. 6.8(a). The electron affinity and the work function of LiNbO$_3$ have been reported by Strigushchenko$^{[41]}$. Though the exact band values of the sample under test might differ from them, they should not affect our conclusion since only qualitative analysis is made. From Fig. 6.10(a) it is concluded that when a MFS structure is formed two Schottky barriers are formed as in Fig. 6.10(b). One is at the metal electrode and film interface, with a barrier height of 5.2eV, and the other is at the film and Si substrate interface with a barrier height of 3.95eV. A detailed discussion of the conduction current behavior of the asymmetric ferroelectric capacitor has been given by Zheng et.al. $^{[42]}$ who concludes that in positive bias region, the conduction is controlled by the bottom electrode barrier height, and in the negative bias region the conduction is controlled by the top electrode barrier height. As the bottom barrier height is smaller than the top barrier height, the conduction current in the positive bias region will be bigger than that in the negative bias region.

From the above discussion, the Schottky barrier conduction mechanism is suggested to be the dominant conduction mechanism for this sample within region I and III.
FIGURE 6.12 The schematic view of the MFS structure band diagram: (a) before contact and (b) after contact with no bias
Chapter 7

Conclusion and Future Study

The motivation for studying the MFS structure is to integrate it to make a MFSFET memory cell with a non-volatile non-destructive readout. Therefore the desired structure should have a large polarization density, low leakage current, appropriate programming voltage and stable switching. From our study of the P-E, C-V, P-S and I-V behaviors of the LiNbO₃ MFS structure, it is believed that this structure is a promising candidate for this kind of application.

Though the device under test breaks down before it saturates, the remnant polarization as large as 17μC/cm² is obtained when the bias is 10V. The precise calculation of how much drain current readout difference can be done according to Miller's theory [16], but it is too complex and beyond the scope of this thesis. A rule of thumb is 0.5μC/cm² polarization charges can introduce a 30μA drain current difference. It is obvious that 17μC/cm² is large enough to get a good readout.

The two competitive charge controlled behaviors are studied with the C-V measurement and it is found that the polarization charge is the dominant mechanism in controlling the ferroelectric semiconductor interface property. Also, the memory window of 1.6V is recorded.

To make the MFSFET feasible in IC technology, the programming voltage cannot be larger than 5V. As shown above, LiNbO₃ has enough polarization density under a
voltage bias of 10V. However, this is for a film with a thickness of 0.34μm. By further decreasing the film thickness, it is expected that the necessary programming voltage can go below 5V.

The leakage current behavior is studied and it has a magnitude at the micron ampere level. This leakage level is small enough for kilobytes memory applications, but further improvement should be made to make it reliable for higher density memories. Therefore, its conduction mechanism is analyzed. Due to lab experimental limitations and limited time, the temperature and thickness dependences of the leakage current haven’t be studied. However, the nice fit between the experimental data and the theory prediction of Schottky barrier conduction suggests that this interface-controlled conduction is the main factor leading to the leakage current for our sample in region I and III. If this conduction mechanism is true with this electric field region, it is expected that changing the Schottky barrier height, the leakage current could be reduced.

The switching transient curve demonstrates that the switching time is about 80~100ns and that it decreases with the increasing electric field. This fast switching time is desirable for memory application.

The charge retention after the switching will be an important research direction for future study since the retention time for our current sample is too short for memory applications. To improve the retention behavior performance, the depolarization field inside the film should be studied in detail and should be reduced as much as possible.
This can be done by analyzing the geometry effects on the MFS capacitors.

Another possible research direction is to study the doping effect. Doping can be applied either in LiNbO$_3$ thin films during processing or by increasing the doping level of the substrate to reduce the screening length. For doping in LiNbO$_3$ thin film, the most noticeable effect is the change of the band structure. This may directly change the Schottky barrier height and thus change the conduction behavior. E.g. according to the proposed back-to-back Schottky barrier model for explaining the I-V curve, if the work function of LiNbO$_3$ is changed with doping, the Schottky barrier height at the bottom interface may increase. This will decrease the positive bias conduction current. Doping can also be used to change the ferroelectric switching behavior. Many work have been done on PZT and BST, but few work are reported on LiNbO$_3$.

According to the discussion from Fig. 6.5, the Sawyer-Tower circuit for the P-E measurement can be revised to measure the relaxed remnant polarization by changing the applied waveform. A triangle pulses chain can be used as in Fig. 6.11. A time interval $\Delta t$ is allowed between pulses for relaxation, so both the remnant polarization and relaxed polarization can be measured. Also, the frequency dependency of the P-E curves should be studied, since for real applications the device often works within high frequency range. Note that high frequency may increase the coercive field and change the remnant polarization density [44]. This makes it more difficult to find the trade-off between a
proper switching electric field and a right thickness of the film that can hold enough remnant polarization for good information readout.

\[ V(t) \]

\[ \Delta t \]

**FIGURE 7.1 The pulse chain for measuring the relaxed remnant polarization**

In summary, the electrical properties of our LiNbO\(_3\) thin films in the MFS structure demonstrate that this material has a large polarization charge density, a fast switching time, and low leakage current. This shows that this MFS capacitor has the potential to be integrated into a MFSFET memory. Further work should be stressed on the retention behavior, the film thickness dependence effect and the doping effect.
References


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Appendix: Glossary of Symbols

\( A^* \)  
Effective Richardson constant

\( \Delta E_{ai} \)  
Activation energy of ions

\( \Delta E_{ue} \)  
Activation energy of electrons

\( \phi_{Bt} \)  
Trap barrier height

\( \Psi_s(V) \)  
Surface potential of the semiconductor substrate

\( \chi \)  
Electron affinity

\( \alpha \)  
Activation field

\( \varepsilon_{oo} \)  
Optical dielectric constant equal to the square of the refractive index

\( \phi_{B0} \)  
Shottky barrier height

\( \varepsilon_d \)  
Dynamic dielectric constant used in calculatin \( \Delta \phi \)

\( \varepsilon_{DC} \)  
Static dielectric constant

\( \phi_m \)  
Metal work function

\( \varepsilon_r \)  
Relative dielectric constant

\( A \)  
Area of electrode

\( \text{BST} \)  
Barium Strontium Titanate \( \text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3 \)

\( C_{acc} \)  
Capacitance in accumulation region

\( C_i \)  
Insulator film capacitance in MIS structure

\( d \)  
The film thickness

\( e \)  
Charge of an electron

\( E_c \)  
Coercive field

\( \text{FeDRAM} \)  
Ferroelectric Dynamic Random Access Memories

\( \text{FeNVRAM} \)  
Ferroelectric Nonvolatile Random Access Memory

\( J \)  
Leakage current density

\( m^* \)  
Effective mass

\( \text{MFSFET} \)  
Metal Ferroelectric Semiconductor Field Effect Transistor

\( \text{MIS} \)  
Metal-Insulator-Semiconductor

\( \text{MOSFET} \)  
Metal Oxide Semiconductor Field Effect Transistor

\( P_r \)  
Remnant polarization density

\( P_s \)  
Saturation polarization density

\( \text{PZT} \)  
Lead Zirconium Titanate \( \text{PbZr}_x\text{Ti}_{1-x}\text{O}_3 \)

\( Q_f \)  
Fixed oxide charge

\( Q_{it} \)  
Interface trapped charge

\( Q_m \)  
Mobil ionic charge

\( Q_{ot} \)  
Oxide trapped charge

\( \text{SBT} \)  
Strontium Bismuth Tantalate \( \text{SrBi}_2\text{Ta}_2\text{O}_9 \)

\( t_s \)  
Switching time constant

\( V_{flat} \)  
Flat-band voltage

\( \Delta \phi \)  
Shottky barrier lowering due to Shottky effect