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RICE UNIVERSITY

Electrical Transport in a Single-Electron Transistor Coupled to a Tunable Environment

by

Wei Lu

A Thesis Submitted in Partial Fulfillment of the Requirements for the Degree Master of Arts

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ABSTRACT

Electrical Transport in a Single-Electron Transistor
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A novel model system is developed to study the effects of the environment on transport properties of a superconducting single-electron transistor (S-SET). The impedance of a two-dimensional electron gas (2DEG) 50 nm below the sample surface serving as the environment can be tuned in situ. A quantum dot is readily formed in the 2DEG. Josephson tunneling processes in the SET are suppressed and quasiparticle tunneling processes are enhanced as the 2DEG is confined. Important energetic parameters of the SET such as the charging energy $E_c$ and superconducting energy gap $\Delta$ remain almost unchanged in this process.
Acknowledgments

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1 INTRODUCTION

Single-electron tunneling processes have recently invoked a lot of interest for both reasons of fundamental scientific interest [1] and potential technological application [2]. In principle devices based on single-electron tunneling will function even if fabricated out of single molecules, and in fact single-electron tunneling has been observed in structures whose dimensions are only a few tens of nanometers [3,4]. Because tunneling is inherently quantum-mechanical, it is ideally described by a Schrödinger equation containing the internal degrees of freedom of the nanostructures involved. In the real world however, no system exists in isolation. A more accurate description of tunneling must take into account external degrees of freedom, which are often termed "the environment." The environment usually involves many degrees of freedom and is often dissipative. A large body of theoretical work has been devoted to incorporating such dissipative phenomena in a conservative Hamiltonian description [5–7]. The interaction between quantum variables and their environment remains a topic of considerable interest today, in connection with the fields of quantum computation [8,9] and mesoscopic transport [10].

Previous studies of the effects of the environment have often involved system of either normal metal or Josephson tunnel junctions [11]. While in many experiments care was taken to ensure that the environment was well-characterized [12–14], and some variation was achieved [15], in general dissipation was not a tunable parameter. Recently, however, it has been demonstrated that well-characterized experimental systems can be fabricated in which some part of the environment can be tuned in situ [16]. Moreover, since tunneling is extremely sensitive to the nature of its environment, tunnel junctions also provide a form of sensor for investigating the electrodynamic
structure of their surroundings. This capability should allow for the study of the
impedance and energetic structure of nanostructures at very low power levels (typ-
ically sub-picowatt) without direct electrical contact, only capacitive coupling. The
results of such measurements can provide information of interest to numerous dis-
ciplines involved in nanoscale science and technology.

The structure on which we have based our investigation consists of an island linked
to macroscopic leads by two Al/AlO$_x$ tunnel junctions, and surrounded by several
gates which control the tunneling of individual electrons. Such a device is referred to
as an “single electron transistor” (SET). The substrate on which the SET is fabricated
contains a GaAs/Al$_x$Ga$_{1-x}$As heterostructure. A layer of two-dimensional electron
gas (2DEG) forms between GaAs and Al$_x$Ga$_{1-x}$As layers [17] about 50 nm below
the surface, and serves as an environment which is strongly coupled to the SET. By
applying sufficient negative voltages on the gates surrounding the SET, the 2DEG
beneath them can be depleted and the impedance of the environment can therefore
be tuned \textit{in situ}. Corresponding changes in the transport properties of the SET
may then be observed. The 2DEG can be further confined to form a quantum dot.
By measuring the dc \textit{I-V} characteristics of the SET, we may also obtain information
about the dot without direct electrical contact to it.

A brief overview of the structure of this thesis is as follows:

In \textbf{Chapter 2} we will discuss the theory of single-electron tunneling. We will
present a very simple semiclassical description of the behavior of a simple SET in the
normal state, and extend the theory to an SET in the superconducting state. We will
then briefly discuss the effects of the environment on transport properties of the SET
and the model system we designed to study those effects. In the end, we will discuss
the case of an SET coupled to a quantum dot. i. e., a double dot system.

In Chapter 3 we will discuss the experimental techniques used in obtaining our results. These include sample design, sample fabrication, cryogenic techniques, low-noise electronic techniques, and data acquisition techniques.

In Chapter 4 we present the electrical measurements of the SET for different environmental conditions. We will first discuss results for the case of an unconfined 2DEG, then examine the changes in the SET transport properties as the 2DEG is gradually confined, and ultimately becomes a quantum dot.

Finally in Chapter 5 we present our conclusions and discuss some possible future experiments.
2 THEORETICAL OVERVIEW

In this chapter we give a theoretical overview of the experiment. The discussion is organized as follows: Section 2.1 discusses the theory of a single SET, in both the normal and superconducting states. Section 2.2 describes quantum dots and their formation in a semiconductor heterostructure. Sections 2.3 and 2.4 discuss the effects of the environment on the SET, and the model system we designed to study those effects, respectively. In Section 2.5 we will give an description for an extreme case when the environment consists of a quantum dot. All of the discussion in this chapter is in the $T = 0$ limit.

2.1 Theory of SET

Consider a system which consists of two ultrasmall tunnel junctions driven by a transport voltage $V$, with a gate capacitor coupled to the island between the junctions, as illustrated in Fig. 1. This forms a single electron transistor (SET). The first observation of single charge tunneling in microfabricated samples by Fulton and Dolan [18] was made in a similar structure.

The island of the SET usually contains thousands of electrons, and the energy spectrum can be disregarded. We can then treat the SET semiclassically.

2.1.1 SET in Normal State

Suppose that the SET is in the normal state, and that $R_T$ and $C$ denote the resistance and capacitance of a tunnel junction. In what follows, we assume that the following two conditions are satisfied. First, we assume the lifetime due to tunneling $\tau_r = R_TC$ is much larger than the time uncertainty $\Delta t$ associated with the Coulomb
Figure 1: The SET consists of two tunnel junctions in series forming an island. The offset charge on the island and therefore its electrostatic potential is varied by the gate voltage $V_g$ through the capacitance $C_g$. The transport voltage $V$ induces a net flow of charge through the device, the value of current $I$ being controlled by $V_g$.

energy $E_C = e^2/2C$. where $\Delta t \sim \hbar/2E_C$. This ensures that the wave function of an excess electron on the island will be localized there. Combing these two expressions, we obtain

$$R_T \gg R_K$$

(1)

where $R_K = \hbar/e^2 \approx 25.8 \text{ k}\Omega$ is the resistance quantum. Second, we assume the island is small enough and the temperature low enough that the energy $E_C$ is large compared to the ambient thermal energy $k_B T$, i.e.

$$E_C \gg k_B T$$

(2)

Under these conditions, the system is in the well-known Coulomb-blockade regime [19], and the excess charge on the island is well defined. When an electron tunnels onto the island, it will change the charge of the island by $e$, thereby increasing the potential of the island. The change in the island potential due to the presence of the excess
electron can be large enough to affect the tunneling rate of other electrons. For the system illustrated in Fig. 1, the electrostatic energy difference due to a transition from \( n \) to \( n + 1 \) excess electrons as a consequence of tunneling across the first junction is found to be

\[
\Delta E_1 = \frac{e[\left( C_2 + \frac{1}{2}C_g \right)V - C_g V_g + ne - \frac{e}{2}]}{C_\Sigma}
\]

where

\[
C_\Sigma = C_1 + C_2 + C_g
\]

is the capacitance of the island. In Eq. (3) the gate voltage \( V_g \) only appears in the combination \( C_g V_g - ne \), so that \( C_g V_g \) acts effectively as an offset charge \( Q_0 = eV_g \) on the island which can be controlled by the gate voltage \( V_g \).

For an electron to tunnel onto the island through junction \( i \) \((i = 1 \text{ or } 2)\), the transition must be electrostatically favorable, requiring \( \Delta E_i > 0 \). A straightforward analysis of Eq. (3) then gives the tunneling condition

\[
\kappa_i eV(Q_0) \geq 2E_C[(-1)^{i-1}(\frac{Q_0}{e} - n) + \frac{1}{2}]
\]

where

\[
\kappa_i = 1 - (C_1 + C_g/2)/C_\Sigma
\]

is the fraction of the applied bias voltage appearing across junction \( i \), and

\[
E_C = e^2/2C_\Sigma
\]

is the Coulomb charging energy of the island. This energetic requirement is illustrated in Fig. 2, in which an electron can tunnel onto the island thereby changing \( n \) from 0 to 1 only when \( eV \) is larger than the energy difference between the \( n = 1 \) and \( n = 0 \) states. This energy difference can be tuned by adjusting \( V_g \) and hence \( Q_0 \).
Figure 2: Schematic illustration for single-electron tunneling conditions. The parabolas represent the energy for \( n = 0 \) and \( n = 1 \) states vs offset charge \( Q_0 \), respectively. Tunneling processes can only happen when the energy provided by the bias \( eV \) is larger than the energy difference between the initial and final states. Adjusting \( Q_0 \) will adjust this energy difference.

By considering tunneling events on and off the island through each junction, it can be shown [11] that the state with \( n \) electrons on the island of the SET is stable with respect to tunneling across the first and second junctions for voltages satisfying

\[
e(n - \frac{1}{2}) < C_g V_g + (C_2 + \frac{1}{2} C_g)V < e(n + \frac{1}{2})
\]
\[
e(n - \frac{1}{2}) < C_g V_g - (C_1 + \frac{1}{2} C_g)V < e(n + \frac{1}{2})
\]

respectively. Hence, in the \( V_g-V \) plane rhombic-shaped regions form along the \( V_g \) axis within which the island is charged with a fixed number of excess electrons, as illustrated in Fig. 3. Inside these rhombi all transitions are suppressed by a Coulomb blockade and no current flows through the device.
Figure 3: The stability diagram of a normal state SET with $2C_2 = 10C_g = C_1$. The transistor conducts only outside the rhombic-shaped regions. Inside these regions, there is a constant number $n$ of electrons on the island.

Figure 4: Coulomb blockade oscillations of an SET for a fixed bias voltage $V < e/C_\Sigma$. No current flows through the SET when the number of electrons on the island $n$ is stable.
If we apply a fixed bias voltage $V < e/C_c$, and change the offset charge on the island by sweeping the gate voltage $V_g$ we will get no current when the charge is located inside one of the rhombi and some current when the charge is outside the rhombi. This phenomena gives rise to the well-known "Coulomb blockade oscillations" as illustrated in Fig. 4.

2.1.2 SET in Superconducting State

Ultrasmall Al/AlO$_x$ barriers (lateral dimensions below 100 nm) are commonly used to serve as the tunneling junctions due to the high quality oxide film which naturally forms on Al. The leads and central island of the SET are then therefore both Al, which will become superconducting at sufficiently low temperatures. For an SET with both superconducting leads and a superconducting island (S-SET), the transport occurs via both Cooper pair and quasiparticle tunneling processes [20, 21]. There are three important energy scales in this case: the superconducting energy gap $\Delta$, the charging energy $E_C$ and the Josephson coupling energy $E_J$ given by the Ambegaokar-Baratoff relation [22]:

$$E_J = \hbar \Delta / 8e^2 R$$  (9)

In this thesis we are concerned with the limit $E_J \ll E_C$, for which the number of excess electrons $n$ on the island is well-defined, and the system is governed by the charging energy of the island.

Fig. 5 shows the energetic requirements for tunneling processes for an S-SET. The states with an odd number of electrons on the island are of energy $\Delta$ higher than those with an even number of electrons, due to the increased free energy associated with the unpaired electron on the island [23–25]. In a Cooper pair tunneling process,
two electrons tunnel at once and change the number of electrons on the island by 2. As shown in Fig. 5, a Cooper pair tunnels onto the island and changes the energy from an initial state of \( n = 0 \) to a final state of \( n = 2 \). Since Cooper pair tunneling processes are dissipationless, the energy provided by the bias \( eV \) must be exactly the same as the energy difference between the initial and final states. For a single electron to tunnel through a junction, however, enough energy must be provided to compensate for the superconducting energy gap \( \Delta \), and to overcome the change in the charging energy. Normally, the energy associated with pair breaking is provided by the bias voltage \( V \), so this term need to be added when calculating the tunneling.

Figure 5: Schematic illustration of energetic requirements for Cooper pair and quasiparticle tunneling processes. A cooper pair tunnelling process (double line) will change \( n \) by 2, while a quasiparticle tunneling process (single line) changes \( n \) by 1 and must overcome both \( \Delta \) and the change in charging energy.
rules. Pair breaking can also be caused by other sources such as thermal excitation and fluctuations in the environment (which we will discuss in the next section). In this case, the extra term is not necessary.

The above rules can be summarized by modifying Eq. (5) to give

$$m \kappa, eV(Q_0) = 2m E_C[(-1)^{l-1} \left( \frac{Q_0}{e} - n \right) + \frac{m}{2}] + q \Delta$$

(10)

where \(m\) is the number of electrons transferred and \(q\) in the number of quasiparticle created by the bias voltage \(V\) in the tunneling process [26].

For Cooper pair tunneling, which we will refer to hereafter as a “J-process”, we transfer two electrons and no quasiparticles, so that

$$m = 2, q = 0$$

For quasiparticle tunneling involving pair breaking due to the bias voltage, which we will refer to hereafter as an “e-process”, when a single electron tunnels, a Cooper pair must be broken, and a “quasihole” is left on the other side of the junction, so we have

$$m = 1, q = 2$$

For quasiparticle tunneling in which pair breaking is not due to the bias voltage, which we will refer to hereafter as a “q-process”, we have

$$m = 1, q = 0$$

Notice that Eq. 10 gives a threshold for quasiparticle tunneling, but a resonant condition for Cooper pair tunneling.

The first two transitions have been studied extensively [26, 27], and are expected at very low temperatures. In many studies of S-SET transport, the fluctuations due
to the environment and the temperature are both very small. The tunneling rate for
the q-process is therefore very small and this process is neglected. We will also refer
to this process as the "anomalous" quasiparticle tunneling process.

Also from Fig. 5, we can see that in a system for which the q-process rate is small,
and at low biases $eV < \Delta$ so that e-process is also not allowed, only the states with
even number of electrons on the island will be populated. The $I-V$ characteristics
of the S-SET are then expected to be $2e$ periodic since only J-process is important
under these conditions. On the other hand, the lack of $2e$ periodicity at low biases
indicates the presence of a large q-process rate.

2.2 Theory of Quantum Dot

A quantum dot is also an SET in that it also consists of two tunnel barriers
and a central island. Unlike a metal SET, a quantum dot usually contains only a
few hundred or thousand electrons on the island due to the low sheet density and
small effective mass associated with the semiconductor forming the island. As a
result, energy level structure of the electron states is present along with the normal
Coulomb blockade phenomena.

2.2.1 2DEG in GaAs/AlGaAs Heterostructure

The quantum dot in our system is formed by lateral confinement of a two-dimensional
electron gas (2DEG) present in a GaAs/Al$_x$Ga$_{1-x}$As heterostructure, created by grow-
ing a layer of Al$_x$Ga$_{1-x}$As on top of a GaAs substrate using molecular beam epitaxy
(MBE) [28]. Typically, the Al mole fraction $x = 0.3$. The band-bending diagram
of such a structure is illustrated in Fig. 6. A conduction band offset of about 0.3 V
forms at the GaAs/AlGaAs interface due to the larger bandgap of AlGaAs. Further-
Figure 6: Band bending diagram of a modulation doped GaAs/Al$_x$Ga$_{1-x}$As heterostructure. A 2DEG is formed in the undoped GaAs at the interface with the $n$-type doped AlGaAs.

more, the AlGaAs layer is usually $n$-doped. As a result, in equilibrium the Fermi level at the interface lies inside the conduction band of the GaAs layer, which assures that electrons will be present at the interface even at $T = 0$. These electrons are confined by the potential well formed at the interface, and by the attractive electrostatic potential due to the positively charged ionized donors in the AlGaAs layer. To reduce scattering from these donors, the doped layer is separated from the interface by an undoped AlGaAs spacer layer. Two-dimensional subbands are formed as a result of confinement perpendicular to the interface and free motion along the interface. Usually, only a single two-dimensional subband (associated with the lowest discrete confinement level in the well) is populated, which gives us the so-called “two dimensional electron gas”.

If metal gates are fabricated on the surface, and we apply a large enough ($\sim 0.3$ V)
negative bias on the gates, the 2DEG beneath them will be depleted. We can think this of either as repulsion from the negative biased gates or as lowering of the Fermi level in GaAs. Increasing the voltage will deplete the 2DEG in a larger region surrounding the gates due to fringing fields.

2.2.2 Quantum Point Contacts and Quantum Dot

In a split gate scheme [29, 30], a negative voltage is applied on two gates pointing toward each other, as illustrated in Fig. 7. Wide 2DEG regions under the gate are depleted, leaving a narrow channel under the gap. If the gap is small enough, typically < 250 nm, and the voltage large enough, the 2DEG in the channel will split itself into a series of one-dimensional subbands, forming a so called quantum point contact (QPC) [31, 32]. The conductance $G$ of such a point contact is quantized due to the discreteness of the 1D levels [33]. Each 1D conductance channel acts as an electron waveguide and provides a conductance of $2e^2/h$, where the factor of 2 arises from spin
Figure 8: Conductance of a quantum point contact as a function of the gate voltage. The conductance is quantized due to the discrete 1D conduction states.

degeneracy. Thus we get

$$G = \frac{2e^2}{h}N = 2G_0N$$

where $N$ is the number of subbands occupied, and $e^2/h$ is usually referred to as $G_0$, the conductance quantum. Increasing the gate voltage will depopulate the 1D subbands, thereby decreasing $N$. Fig. 8 shows a schematic illustration of point contact conductance $G$ vs. gate voltage $V$.

A quantum dot can by formed by putting two narrow split gates in series with another pair of more widely spaced gates, as illustrated in Fig. 9. When sufficiently negative voltages are applied on the gates, the 2DEG will form an island in the center, while the two point contacts serve as tunnel barriers with $N \ll 1$ in Eq. 11 so that condition $R_{qpc} \gg R_K$ is satisfied.
Figure 9: Formation of a quantum dot using three pairs of gates. The two quantum point contacts serve as tunnel junctions while the island is formed by depletion of electrons under the central gates.

2.3 Effects of the Environment

When electrons tunnel through a normal junction, they can exchange energy with the external environment, by either emitting or (for non-zero temperature) absorbing photons. The probability $P(E)$ of emitting or absorbing a photon can be calculated [34], and is related to the real part of the total impedance $Z_r(\omega)$ perceived by the tunneling electron. The distribution function $P(E)$ in turn determines the tunneling rate (and therefore the current) through the junction. Note that the relevant frequency scale is $eV/h$, where $V$ is the voltage across the junction and $e/h = 242$ THz/V, so that measurements of the dc $I-V$ characteristics are naturally sensitive to the nature of the surrounding electrodynamic environment at very high frequencies.
Similar effects occur in Josephson tunnel junctions. The frequency associated with a voltage $V$ is now $2e/h = 484$ THz/V. The charge $Q$ on the junction and the superconducting phase difference $\varphi$ across it are conjugate parameters and satisfy an uncertainty relationship $\Delta \varphi \Delta Q \geq 2e$: in the proper parameter range, competition between phase and charge fluctuations can determine the nature of transport through a junction. Once again a function $P'(E)$ describes the probability of energy transfer and in turn determines the tunneling rates for Cooper pairs.

For an S-SET consisting of two Josephson junctions, a model Hamiltonian describing the system is given as [21, 25]

$$
H_0 = \sum_{Q,\overline{Q}} \left\{ \left[ \frac{(Q + Q_0)^2}{2C_\Sigma} - \frac{1}{2} Q V \right] |Q, \overline{Q}\rangle \langle Q, \overline{Q}| - \frac{E_j}{2} \sum_{\pm} \sum_{\pm} |Q \pm 2e, \overline{Q} \pm 2e\rangle \langle Q, \overline{Q}| \right\}
$$

where $Q$ is the electron charge on the island and $\overline{Q}$ is the total charge which has passed through the SET. In this Hamiltonian, only Josephson tunneling processes are considered. The effects of the environment and quasiparticle tunneling will be accounted for as perturbations.

An external impedance gives rise to two effects. First, it may cause incoherent Cooper-pair transitions, whose rate is given by

$$
\Gamma_{i-f}^{\text{env}} = \frac{1}{\hbar^2} |\langle \Psi_f | \overline{Q}/2 | \Psi_i \rangle|^2 \frac{2ReZ(\varepsilon_{if}/\hbar)\varepsilon_{if}}{1 - \exp(-\varepsilon_{if}/k_B T)}
$$

Second, it may give rise to photon assisted tunneling given by

$$
\Gamma_{i-f}^{\text{qp}} = \frac{1}{\hbar^2 R_t} \frac{R_e}{2R_K} \frac{R_e}{k_B T_e} \frac{2\Delta}{2\Delta - \varepsilon_{if}} e^{-(2\Delta - \varepsilon_{if})/k_B T_e}
$$

where $Z(\varepsilon_{if}/\hbar)$ in Eq. 13 is the impedance of the environment at $\omega = \varepsilon_{if}/\hbar$ and $R_e$ in Eq. 14 is the resistance of the environment. We can see that the transport properties of the SET are again sensitive to the electrodynamics of the environment.
On the other hand, relatively little work has been done on this problem experimentally, in part because a tunable environment is hard to achieve. In most experiments to date, the single most important source of dissipation was the macroscopic leads coupling the junctions to the room temperature measurement electronics. Such leads can be modeled as transmission lines, with some distributed resistance, inductance and capacitance per unit length [35, 36]. Because the impedance of free space is small (337 Ω), unless great care is taken the leads typically present a low impedance to the junctions at microwave frequencies, making the observation of how tunneling properties change with the environment difficult.

2.4 Model System

In order to address this problem, we have developed a model system as illustrated in Fig. 10. In this system, a superconducting SET (S-SET) is capacitively coupled and closely adjacent to a layer of 2DEG in the substrate about 50 nm below the surface. The impedance of the 2DEG can be controlled by adjusting the voltage on the gates. The island of the SET is coupled to ground through both the junctions and the 2DEG. The capacitance $C_{2\text{DEG}}$ between the 2DEG and the SET is large compared to the junction capacitances $C_i$ in our system, so the effective environmental impedance perceived by the tunnel junctions is dominated by the impedance of the 2DEG.

There are several advantages in this model system:

- The impedance of the 2DEG, hence the environmental impedance perceived by the SET, can be tuned in situ. We can therefore observe changes in the transport properties of the SET as the environment changes.

- The 2DEG may be readily confined to form a quantum dot. Transport through
Figure 10: Lumped-element circuit for the model system. A central island is isolated from the macroscopic leads (white rectangles) of impedance $Z_L(\omega)$ by tunnel junctions (paired rectangles) of resistance $R$ and capacitance $C$. The island is in turn coupled by a capacitance $C_{2DEG}$ to an external environment (grey rectangle) with impedance $Z_{env}(\omega)$, which can be readily varied.
the SET is sensitive to the high-frequency electrodynamic properties of the quantum dot, which are of great scientific interest in and of themselves.

- The electronic energy levels in the quantum dot can also be tuned, both in terms of spacing and level width, allowing adjustment of the energetic structure of the environment presented to SET.

### 2.5 SET Coupled to a Quantum Dot

If the 2DEG is confined into a quantum dot, the system is then effectively a strongly coupled double dot system, as illustrated in Fig. 11, where $C_s$ is the capacitance between the gate and the SET, and $C_d$ is the capacitance between the same gate and the dot.

Changing the gate voltage $V_g$ will change the effective offset charges on the islands of both the SET ($Q_{0s}$) and the dot ($Q_{0d}$). A calculation of $Q_{0s}$ and $Q_{0d}$ gives:

$$Q_{0s} = C_s V_g + (C_d V_g - n_2 e) \frac{C_{2\text{DEG}}}{C_d + C_3 + C_4 + C_{2\text{DEG}}}$$  \hspace{1cm} (15)

$$Q_{0d} = C_d V_g + (C_s V_g - n_1 e) \frac{C_{2\text{DEG}}}{C_s + C_1 + C_2 + C_{2\text{DEG}}}$$  \hspace{1cm} (16)

where $n_1$ and $n_2$ are the number of electrons on the island of the SET and the dot, respectively.

Besides the induced offset charge $C_s V_g$ due to the direct coupling between the gate and the SET, $Q_{0s}$ in Eq. 15 is also affected by $N_2$, which is in turn changing as $C_d V_g$ changes in Eq. 16. The effects of changes in $N_2$ cannot be neglected in the strongly coupled case, i.e., when $C_{2\text{DEG}}$ is large. Thus we will see a beating effect between the two offset charges in the current through the SET as we sweep $V_g$. If $C_s \sim C_d$, 

Figure 11: An SET coupled to a quantum dot through a capacitance $C_{2DEG}$. The dot and SET are biased independently by voltages $V_1$ and $V_2$. The gate capacitances $C_s$ and $C_d$ can have significantly different values.
both \( N_1 \) and \( N_2 \) change at roughly the same rate, and little information about the properties of the SET can be determined from the measurements.

However, in a limit \( C_s \ll C_d \), \( N_1 \) will change much more slowly than \( N_2 \) due to the much weaker coupling to the gate. Thus the \( C_s \) and \( N_1 \) terms in Eq. 16 can be neglected, and \( Q_{0d} = C_d V_g \) to first order. \( i.e. \), the dot behaves like an isolated SET and \( N_2 \) will in general change in phase with \( C_d V_g \). Since \( N_2 \) can only be an integer while \( C_d V_g \) changes continuously, the combination of these two terms only adds an oscillation in the offset charge in Eq. 15. As a result, if we perform Coulomb blockade oscillation measurements discussed in Section 2.1.1 in this limit, curves similar to the one illustrated in Fig. 4 are still expected for the dot. As for the SET, instead of a smooth current curve in Fig. 4, we expect curves similar to the one illustrated in Fig. 12. The larger period in the current is caused by the direct gate modulation.

![Graph showing Coulomb blockade oscillations through the SET.](image)

Figure 12: Coulomb blockade oscillations through the SET. The larger period in \( I \) is caused by offset charge change due to direct coupling from the gate, modulated by the smaller period oscillations due to offset charge change in the Dot.
from $C_s$, while the smaller period is due to the changes in the offset charge of the dot. Information about the transport properties of the SET can still be determined from the envelope of the oscillations in the current curve.
3 DESCRIPTION OF EXPERIMENT

This chapter describes the design, fabrication and measurement of the sample. Section 3.1 discusses the sample design and gives an overview of the sample fabrication. Sections 3.2, 3.3 and 3.4 describe in detail the important fabrication steps, including making Ohmic contacts, electron beam lithography, alignment of the Al and Au layers, development, and metallization. Sections 3.6 and 3.5 detail the set-up for the electrical measurements and refrigeration, respectively.

3.1 Sample Design

The sample investigated in our experiment is illustrated schematically in Fig. 13. The small gates and junctions are connected to corresponding pads through a series of leads with sizes increasing from 1 \( \mu \text{m} \) to \( \sim 30 \ \mu \text{m} \). The sample will then be connected to macroscopic wires at the pads, whose sizes are about \( 250 \times 250 \ \mu \text{m}^2 \). Fig. 14 shows a closer look at the sample. The tunnel junctions forming the SET are produced by a standard shadow evaporation technique [37]. As shown in the cross-sectional view, two Al layers overlap each other: between them is an oxide layer serving as the tunnel barrier. The sizes of the junctions in this sample are about 50 nm \( \times \) 50 nm, and the thickness of the oxide layer is about 10 Å.

We start with a small piece (\( \sim 2 \ \text{mm} \times 3 \ \text{mm} \)) of GaAs containing a layer of high mobility 2DEG about 50 nm below the surface. The material is provided by Dr. Gossard's group at UC Santa Barbara. After placing Ohmic contacts on the four corners of the sample to make electrical connections to the 2DEG, we use electron beam lithography to fabricate Au gates first. Different 2DEG confinement can be achieved by adjusting the voltages on the gates, as discussed in Chapter 2.
Figure 13: Schematic illustration of the sample, showing the ohmic contacts, Au gates and macroscopic pads for making contact to the SET.
Figure 14: Expanded view of the center of the sample, showing the Al/AlO_x tunnel junctions, the depletion of the 2DEG, and relevant length scales.
After the Au deposition and liftoff, the SET is fabricated by another electron beam lithography step. The alignment of the SET to the gates is critical: as illustrated in Fig. 14, the SET must be located in the middle of the Au gates precisely. We must also run Al leads through the gates defining the quantum point contacts without causing shorts, with spacings of the split gates being only about 150 nm.

A reliable technique for aligning these two layers has been developed to solve those problems. An electron micrograph of a test sample is shown in Fig. 15. The tunnel junctions are visible as the overlaps between the vertical leads and the central island. Alignment with an error of <30 nm has been successfully achieved.

Note the intentional asymmetry of the central island of the SET shown in Fig. 15. Because of this asymmetry, the capacitance $C_{sb}$ coupling the SET to the bottom central gate is much smaller than the capacitance $C_{st}$ coupling it to the top gate. When the dot is formed, however, the capacitances $C_{db}$ and $C_{dt}$ coupling the SET to its gates are nearly equal and not very different from $C_{st}$. We thus have $C_{sb} \ll C_{st} \sim C_{dt} = C_{db}$ This asymmetry gives us some flexibility in controlling the offset charge of the SET:

- Before the dot is fully formed, we use the top gate to modulate the offset charge of the SET. Since $C_{st} \approx 10 \text{ aF}$, the voltage change required to complete an offset charge cycle is about 16 mV. As a result, the conditions of the 2DEG do not change significantly within a period.

- When the dot is formed, since $C_{st} \sim C_{dt}$, changing the voltage on the top gate will change the offset charges of both the SET and the dot by about the same amount, and a large beating effect is expected, as discussed in Section 2.5. In this regime, we use the bottom gate, and since $C_{sb} \ll C_{db}$, curves similar to the
Figure 15: Electron micrograph of a test sample. The white bar at the lower left represents 100 nm. The tunnel junctions are visible as overlaps between the leads and the island. Notice the asymmetric the coupling of the island to the top and the bottom central gates.
one in Fig. 12 are expected.

### 3.2 Ohmic Contacts

Numerous recipes are available which will give ohmic contact to the electron gas in GaAs/Al\textsubscript{2}Ga\textsubscript{1–x}As heterostructures [38]. Here we use one of the oldest and best-known techniques, namely alloyed In.

The exact physical process by which In alloy makes a good ohmic contact is complicated and not well-understood. The InAs formed by the alloyed In may have an electron affinity close to that of GaAs, or a large number of surface states which may pin the Fermi level near the conduction band edge, giving a small barrier height for the InAs/GaAs interface.

Typical steps involved in making ohmic contacts include:

1. Cleave a 2 mm × 3 mm piece of material from the wafer.

2. Clean sample in acetone (ACE) ultrasound for 20 min to remove dust created during the cleaving process. Rinse the sample in isopropanol (IPA), afterwards since ACE evaporates rapidly and may leave residue on the surface. Blow sample dry with a blower.

3. Prepare In on a clean microscope slide by melting In wire (Indium Corp, 99.99%, 0.02 mm) using a soldering iron at 700° F.

4. Press In onto surface of sample using a soldering iron at 600° F.

5. Check “solder” points. It may be necessary to press some extra In down using tweezers.
6. Place sample into tape heater oven. Flush oven with forming gas (20% H$_2$, 80% He) for 10 min. to remove any air from the chamber.

7. Using flow meter, set flow of forming gas to desired rate for baking, typically 70 ml/min.

8. Bake sample at 110° C for 2 min. to remove adsorbed water.

9. Ramp temperature to 400° C; hold at 400° C for 2 min 50 s.

10. Turn off heater. Leave forming gas flowing until sample is cool.

11. Test contacts at 4.2 K.

Baking time is the most important parameter. Since connections need to be made to a very thin electron layer, either too short or too long a bake time will cause failed contacts. If the baking time turns out to be too short, rebaking the sample may help.

The tape heater oven is a home-made 4 x 4 x 4 in$^3$ clear plastic box with gas inlet and outlet ports, and a rubber gasket seal. Two high current (~ 20 A) Cu wire feedthroughs are attached to each end of a 1 x 0.25 x 0.015 in$^3$ nichrome tape, on which the sample is placed. The sample is heated by running a large dc current through the tape, the temperature of which is measured via a thermocouple spot welded to the underside of the tape. The baking is performed in a forming gas atmosphere, in which the H$_2$ acts as a reducing agent, minimizing oxidation of the In and the sample.

### 3.3 Electron-Beam Lithography of Au Gates

Electron-beam lithography of Au gates involves exposing the sample to a high energy electron beam, developing the exposed area, evaporating material on the sample
and liftoff. These processes are illustrated in Fig. 16.

3.3.1 Electron-Beam Resist System

Electron-beam lithography is widely used to produce features with size < 500 nm. Like photo-lithography, e-beam lithography depends on selective exposure of a resist which is sensitive to ionizing radiation. There are two kinds of resists. For a positive resist, exposure to the electron beam has the effect of breaking the bonds holding together the monomers in a resist molecule. The weakened part of the resist can then be removed by a weak solvent (developer) while the unexposed resist remains. For a negative resist, exposure to the electron beam causes bonds (crosslinks) to form between the monomers of different resist molecules, hardening the resist and making the exposed areas insoluble to particular solvents while the rest of the resist can be removed. Positive resists are more widely used. The particular resists we use are polymethylmethacrylate (PMMA) and polymethylmethacrylate mixed with methacrylic acid (PMMA-MAA), both positive resists. The critical energy needed in a volume of positive resist for the resist to be soluble in a developer is called the critical irradiation \( \varepsilon_c \). In practice, the known quantities in an exposure are the beam current density and the exposure time, which in turn determine the number of electrons (the dose) received by the resist. The critical dose \( D_c \) is proportional to \( \varepsilon_c \) for fixed incident electron energy, resist thickness, substrate type and so forth. In practice, the proper dose is determined experimentally.

A bilayer PMMA system [39, 40] is used for fabrication of Au gates. The motivation for using a system of this sort is to produce an undercut resist profile as shown in Fig. 16. The low molecular-weight bottom layer is more sensitive to irradiation than the high molecular-weight upper layer, since fewer bonds must be broken to make the
1) Expose

Electron Beam

resist → low sensitivity high sensitivity substrate →

2) Develop

Metal

3) Evaporation

4) Lift-off

Gates

Figure 16: Schematic illustration of electron-beam lithography process.
lower layer soluble. As a result, more of the lower layer will be removed during the development, leaving some overhanging high molecular-weight resist. An undercut profile facilitates liftoff by minimizing the chance of connection between the metal deposited on the resist and that on the surface of the sample. Liftoff can therefore be accomplished easily with layers of deposited metal up to \( \sim \frac{1}{3} \) of the thickness of the lower resist layer. Bilayer systems also help to reduce the minimum linewidth, which is determined by the exposed area in the upper resist layer. This area is reduced since fewer electrons scattered from the substrate surface reach the upper layer of resist.

The particular bilayer resist we use consists of a lower layer of 495 K PMMA and an upper layer of 950 K PMMA, both 4\% in anisole. The thickness of the lower and upper layers is roughly 100 nm and 100 nm respectively.

A typical sequence of steps in producing a bilayer resist is as follows:

1. Clean sample in ACE ultrasound for 10 min, followed by rinsing in IPA and blow dry (If ohmic contacts have been put on the sample, this step should be skipped, since ultrasound may destroy the ohmic contacts.)

2. Clean a glass pipette in ACE ultrasound for 5 min, followed by rinsing in IPA and blow dry.

3. Apply a drop of 495 K PMMA on the sample. Immediately start the spinner; spin @ 6000 rpm for 40 s.


5. Bake on hot plate @ 180° C for 1 hr.

6. Clean a second pipette for application of the upper layer.
7. Spin on a drop of 950 K PMMA in the same fashion.

8. Check for uniformity of resist.

9. Bake on hot plate @ 180° C for 1 hr.

Immediately starting to spin on the resist is important in creating a uniform resist layer. Furthermore, anisole is a strong solvent for PMMA, and it is possible that the lower layer could be dissolved when PMMA for the upper layer is applied if spinning does not begin immediately.

### 3.3.2 Pattern Generation System

The pattern generation system we use consists of a LEO 440 scanning electron microscope (SEM), a Gateway microcomputer, and pattern generation software and hardware obtained from J. C. Nabit Lithography Systems.

The principle of the NPGS system is illustrated in Fig. 17. We first draw the desired pattern using a CAD program. Different doses and SEM settings (e.g., magnification and beam current) can be allowed for by assigning different parts of the drawing different colors and layers, respectively. A run file is then created by running a program called MRF (make run file). During this step, the specific values of doses and SEM settings are given to the run file. To perform an exposure, NPGS uses a program called PG (pattern generation) to access the information stored in the run file. PG interfaces to the LEO 440 via two 16-bit digital-to-analog converters (DACs) for x and y control of the beam position within the field of view of the microscope and a third line to control the beam blanker. The beam blanker in our system is a pair of parallel plates. When a large enough voltage is applied across the plates, the electron beam is deflected and does not pass through the final aperture. The role of blanking...
Figure 17: A conventional electron microscope converted to an e-beam writer. The microcomputer is equipped with a commercial package, Nanometer Pattern Generation System (NPGS) which interprets CAD drawings on the microcomputer to perform an exposure via control of the scan coils and beam blanker of the SEM.
the electron beam is two-fold: first, by controlling when the beam is blanked. we are
controlling the exposure time and hence the dose received by the resist; second, the
beam must be blanked when it is moved to another place of the sample. so that the
path it follows will not be unintentionally exposed.

3.3.3 Sample Exposure

Sample exposure is a complex process. The major steps are as follows:

1. Ramp up the SEM to the desired voltage (35 kV in this case) and saturate the
   filament.

2. Adjust the settings of the SEM. This includes aligning the gun, aligning the
   final aperture, adjusting the astigmatism and focus of the beam, and setting
   the proper magnification and beam current.

3. Turn on the beam blanker. Move the sample to the desired position.

4. Run NPQS to draw the smallest features.

5. Change the final aperture for patterning of larger features if necessary.

6. Change the corresponding SEM parameters for larger features, such as magni-
   fication and probe current.

7. Run NPQS to draw the larger features.

8. Turn down the filament and shut down SEM.

Usually a much larger probe current and lower magnification are used to draw
the leads and pads than are used to draw the gates, since the leads are much larger
and hence take longer to draw, while patterning them does not require a very fine beam. The final aperture must be changed then since we do not want the large beam current to cause contamination of the smallest aperture used for patterning of the gates. In this sample, three different beam settings and apertures are used for features of different sizes.

After the pattern is drawn, the sample is removed from the SEM and is ready for development. We use a 3 to 1 mixture of isopropanol and MIBK (methyl-isobutylketone) as a developer. The sample is developed in this solvent at 23°C for 60 s, followed by rinsing in IPA for another 30 s. The sample is then blown dry and examined under an optical microscope. The optical microscope cannot resolve features with sizes < 10μm, but it will give us some idea if the larger features have been exposed successfully. If all appears well, it is time to proceed to evaporation and liftoff.

3.3.4 Evaporation

We use Au as the material to form the gates. Au is not superconducting, will not disturb magnet field lines if such a field is applied, and will not oxidize, which make it a popular metal for gate deposition. Au also gives off a strong secondary electron signal, making it easy to see in the SEM and simplifying the alignment process we will talk about later. One problem with Au is that it does not stick to GaAs very well. To solve this problem, a thin layer of Cr is usually deposited first. This combination is very widely used for depositing non-superconducting and non-magnetic patterns.

The metal deposition is performed in a CVC thermal evaporator, which has two evaporating sources. For our samples, the thickness of Cr film deposited is about 20 Å, and the thickness of Au deposited is about 200 Å. The sample is then taken
out and put in ACE for liftoff. The last process usually takes for 4 hrs.

3.4 Fabrication of Al Junctions

Fabrication of Al junctions employs the same e-beam lithography techniques discussed above. This time, however, while the top layer is still 950 K PMMA, as for Au gates, the bottom layer is PMMA-MAA, which has a much higher electron sensitivity than 950 K. In addition, a relatively low accelerating voltage of 20 kV (compared to the 35 kV used for fabricating Au gates) is used so that backscattering of electrons is more prominent, which results in a higher dose in the bottom layer. Due to these measures, a much larger undercut is formed in the bottom layer. In a carefully designed pattern, a suspended “bridge” can be created by exposing two nearby regions. The junctions can then be fabricated by first evaporating Al from one angle, oxidizing, then evaporating a second layer of Al from a different angle, as illustrated in Fig. 18. This technique is called “shadow evaporation”, and is now a standard process used to produce ultrasmall Al/AIO$_2$ junctions [37].

Aligning the SET to the gates is another tricky process. Since the sample has been removed from the SEM for deposition of the gates and resist preparation, physical alignment alone cannot achieve the ~ 30nm alignment accuracy required. In addition, the beam cannot be moved directly to the desired position by viewing the sample in the SEM, because the beam will expose the resist while viewing it. A special program in the NPGS package called “AL” (align) is used to solve this problem. Before AL can be used, a series of alignment marks are fabricated along with the Au gates on the sample, away from the desired location of the SET. A series of windows containing overlays having the same shape as the alignment marks are created in NPGS. By
Figure 18: Major steps involved in fabricating Al/AlO$_x$ junctions. A hanging resist bridge is formed during the e-beam lithography process. Shadow evaporation technique is then used to produce the junction, which is a thin oxide layer sandwiched by two layers of Al evaporated from different angles.
Figure 19: Schematic drawing of the alignment process. Only the areas in the windows are exposed in this process. Adjusting the overlays to the alignment marks allows NPGS to calculate translation to rotation matrices.

running AL, only the areas corresponding to the windows will be exposed. Images of these regions will be shown on the computer screen with the alignment marks located inside the windows if everything is carefully designed. By adjusting the overlays to the corresponding alignment marks, AL will record information such as shifts in the pattern position, rotation and magnification, and create a matrix to compensate for these shifts. This process is illustrated in Fig. 19. NPGS then applies this matrix to the pattern drawing procedure so that the pattern is drawn in the correct position and orientation, and with the correct magnification.
3.5 Refrigeration

All the measurements of this experiment are performed in an Oxford Instruments Model 100 dilution refrigerator, which has a base temperature of 20 mK and is equipped with a 10 Tesla magnet. A good review of the principles of dilution refrigerator can be found in the Oxford manual and Richardson and Smith [41]. Here we give a very brief description of its operation.

If we cool any $^3$He/$^4$He mixture with more than 6% $^3$He concentration to a low enough temperature, the mixture will separate into two phases. One of the phases will be almost pure $^3$He. The other one will be primarily $^4$He, but will still have 6% $^3$He concentration even at $T = 0$. The equilibrium vapor of the $^3$He dilute phase is also almost pure $^3$He due to its higher vapor pressure. These unique properties of $^3$He/$^4$He mixtures provide a means of cooling samples to very low temperatures.

Fig. 20 shows the separation of the two phases. Pumping on the $^3$He dilute phase results primarily in removing $^3$He from the liquid. The equilibrium of the two phases is then broken and $^3$He atoms in the $^3$He rich phase will diffuse across the phase boundary to the $^3$He dilute phase. Latent heat will be absorbed in this process, and samples thermally anchored to the mixture will be cooled down. In practice, the initial cooling is achieved by simple evaporative cooling of the mixture. Phase separation occurs when the mixing chamber temperature reaches 0.86 K. The $^3$He is usually pumped at a fixed higher temperature ($\sim 1$ K), so that there will always be a sufficient vapor pressure, and the cooling can be continued to close to absolute zero. The fridge (called the “insert” in this system) is immersed in a $^4$He bath which is surrounded by a liquid nitrogen jacket.

The sample is mounted on a home-made “tail” screwed into the mixing chamber.
Figure 20: $^3$He/$^4$He mixture separates into two phases at low temperatures. Pumping on the $^3$He dilute phase causes $^3$He to diffuse across the phase boundary, cooling the sample.

Sample heat dissipation must be carefully considered in the low temperature measurements. Heat generated in the sample by electrical measurements can be dissipated both through the on-chip leads and through the substrate. Calculations show that in systems like ours, the heat is mostly dissipated through the on-chip leads. Several heat sinks are screwed on the tail to help thermally anchor these wires. The tail must be carefully designed to be sure there is no large temperature difference between the mixing chamber and the end of the tail where the sample is mounted. The tail is also carefully designed to minimize eddy current heating when the magnet is in use.
3.6 Measurement

3.6.1 Wiring and Filtering

The refrigerator has 24 leads from room temperature down to a connector near the mixing chamber, which is connected to a set of PC boards on the tail with fine manganin wires (0.005 in., California Fine Wire Co.). The connection from the sample to the pc boards are made by a "sandwich technique." An indium dot (a slice of indium wire) is first placed on the on-chip pad. After laying a piece of fine Cu wire on top of the indium dot, another indium dot is placed on top and pressed down using tweezers. To make good low resistance contacts, the surfaces of the pad and the indium dot must be very clean. The first condition is satisfied by making the connection right after liftoff, while the second is satisfied by using the freshly cut surface of the indium slice.

Electrostatic discharge can cause significant problems during wiring. A very small discharge can easily destroy the sample by either burning out the fuse-like leads or punching holes in the thin oxide layer. Numerous measures are taken to reduce the chances of static charge damage. These include:

- Ground all wires before connecting them to the sample.

- Use grounding straps and pads.

- Use antistatic fans (Ion Systems, Z-Stat 6441) and blowers (Simco, AFC-2, PG-5) to neutralize static charges accumulated on the surfaces.

- Use static-safe tweezers.
The wires must also always be grounded after the wiring process until measurements are to be performed.

High frequency noise is a significant concern in these low-temperature, low-signal measurements. Radio frequency or microwave noise can easily heat the sample or contaminate the results of the measurements. To deal with this problem, we have the sample mounted inside a metallic enclosure which is carefully sealed with conductive tape and which serves to block any microwave black body radiation present inside the insert. The fridge itself serves as a shield for radiations from room temperature. Furthermore, all the measurements are performed inside an rf shielded room with an attenuation of more than 100 dB at 1 GHz, and battery powered electronics are used to avoid noise associated with the electrical mains.

The leads must also be carefully filtered to prevent high frequency noise going down them to the sample. In our set-up, each wire is filtered by a "T" filter (Murata Electronics, Inc.) at room temperature and $RC$ and the microwave filters [42] at mixing chamber temperature.

3.6.2 DC Set-Up

DC measurements of the SET characteristics are performed in a symmetrically voltage-biased four-probe configuration, as illustrated in Fig 21. Home-made low-noise voltage and current amplifiers are used to measure the voltage across and the current through the SET. A sensitivity of ~ a few fA in the current and a typical noise of ~ 25 nV/$\sqrt{\text{Hz}}$ in the voltage can be simultaneously achieved for dc signals. The data are recorded by a microcomputer.

Two types of measurements can be performed in this configuration:
Figure 21: Schematic illustration of a dc measurement on the SET. The sweep box generates two symmetric ramping voltages across the SET. The 2DEG is grounded in this measurement.
• We can sweep the bias voltage $V$ of the SET up or down with the gate voltage $V_g$, and therefore $Q_0$ fixed for each sweep, as shown in Fig. 21. Usually a series of $I$-$V$ curves will be measured while stepping $Q_0$ uniformly for consecutive sweeps until the offset charge completes a cycle. This is a good way of studying the SET in one particular condition since information for a variety of bias voltages and offset charges will be obtained.

• We can also use the sweep box to sweep one of the gate voltages $V_g$ while keep the bias voltage $V$ fixed, a measurement similar to Coulomb blockade oscillation measurements. The gate modulation measurement provides better look at some important features since the maximum and minimum current at a given bias voltage can be read directly in each cycle.

The voltage sweeps are produced by a home-made sweep box which generates a dc voltage ramping over different ranges from 12 V to 0.12 mV at various rates. Two channels of output can be swept simultaneously in opposite directions. If both channels are used, the maximum range is doubled. The fixed voltage $V_g$ is produced by a home-made precise voltage generator with a dc voltage fluctuation $< 1 \mu V$.

All these measurements on the SET are performed with the 2DEG grounded, so that no current runs through it, avoiding possible heating of the sample.

3.6.3 AC Set-Up

A small ac signal is used to measure the differential conductances of the quantum point contacts. A typical set-up is illustrated in Fig. 22.

Two Stanford Research SR830 lock-in amplifiers are used in this measurement. An ac signal, typically 50 mV, taken from the “Sync Out” of one lockin is scaled down
by a voltage divider to typically 5 $\mu$V. The frequency of the signal must be carefully chosen to avoid harmonics of the 60 Hz. We usually use 11 Hz in our measurements. The voltage and current are again measured by home-made low noise amplifiers.
Figure 22: Schematic illustration of a differential conductance measurement on the point contacts. The 50 mV signal is scaled down to 5 µV by a 10 Ω + 100 KΩ voltage divider.
4 MEASUREMENTS AND DISCUSSION OF RESULTS

Electrical transport measurements have been performed on the sample for various 2DEG confinements. Section 4.1 discusses tests of sample quality. Section 4.2 and Section 4.3 discuss the transport properties of the SET with no confinement and strong confinement of the 2DEG, respectively. Sections 4.4 and 4.5 present results of how the transport properties of the SET evolve as the confinement of 2DEG changes, from no confinement into the dot regime. Section 4.6 describes the temperature dependence measurements performed to rule out possible effects of sample heating. In Section 4.7 we give some possible explanations for our data.

4.1 Test of the Quantum Dot

One potential flaw of the sample design is that positioning the SET leads between the split gates forming the QPCs and placing the SET island in the center of the dot may affect dot formation. To be sure that this does not occur, we first test the quality of the quantum point contacts using the ac set-up discussed in Section 3.6.3. Both point contacts are tested independently in this measurement, i.e., the left point contact is first tested with the other gates grounded, and a similar test is then performed for the right point contact. The results are shown in Fig. 23. The data for the right QPC have been offset by $2e^2/h$ in this figure for clarity. Up to six plateaus are clearly distinguishable for each point contact, which is a typical result for similar split gate geometries in the absence of an SET. The data therefore indicate that the quantum point contacts are not affected by the existence of the Al leads.
Figure 23: Conductance of the quantum point contacts vs. gate voltage. The upper curve has been offset $2G_0$ for clarity.

The quantum dot can be formed by adjusting the conductances of the two QPCs to about $0.1G_0 - 0.15G_0$, satisfying the condition $G_{qpc} \ll G_0$ while also ensuring the current is not too small to be measured. Voltages corresponding to this conductance value can be read from the curves of $G_{qpc}$ vs. $V_{qpc}$ in Fig. 23. Adequate voltages must also be applied to the central gates to form the dot. In addition, when activating the gates simultaneously, electrostatic coupling between the gates must be considered: the voltage on a given gate changes the effective voltage on the other gates due to the small spacing ($\sim 150$ nm) between them. We measure this effect on the split gates by observing changes in the position of the last plateau in $G_{qpc}$ while varying the voltage of the other gates. Changes in the effective gate voltages can be deduced from these measurements and the proper voltage can be calculated to compensate this effect.

To verify that we can produce a well-formed dot, we have performed Coulomb
blockade oscillation measurements. A typical result is shown in Fig. 24. The capacitance between the gate and the dot can then be calculated from the equation

$$ C = \frac{e}{\Delta V} $$

where $\Delta V$ is the period in the gate voltage corresponding to the change of one electron on the island.

We obtain $\Delta V_t \approx \Delta V_b \approx 5$ mV, giving $C_{dt} \approx C_{db} \approx 32$ aF for the capacitances between top and bottom central gates and the dot, respectively.

4.2 Characterization of SET with 2DEG Unconfined

To study the system, we begin with a simple situation in which all the gates are grounded except the one used to adjust the offset charge on the island. In this situation, the system consists of an SET coupled to a ground plane. The theory in Chapter 2 applies with one modification that another term $C_s$ must be considered in
$C_\Sigma$ and $\kappa_i$, where $C_s$ includes the stray capacitances to all the other five grounded gates and $C_{2\text{DEG}}$, the capacitance to the 2DEG. So now we have

$$C_\Sigma = C_1 + C_2 + C_g + C_s$$  \hspace{0.5cm} (18)

$$\kappa_i = 1 - [C_i + (C_g + C_s)/2]/C_\Sigma$$  \hspace{0.5cm} (19)

and $E_c$ maintains the same form

$$E_c = e^2/2C_\Sigma$$  \hspace{0.5cm} (20)

A series of $I$-$V$ measurements have been performed on the SET with different offset charges $Q_0$ on the island, as discussed in Section 3.6.2. Each sweep takes about 15 min. due to the low cut-off frequency (0.1 Hz) used in the current amplifier to minimize current noise. A false color image of the $I(V,Q_0)$ surface is then produced by plotting the absolute value of the current on a logarithmic scale, as illustrated in Fig. 25. The current varies from $\sim 1$ fA (the sensitivity of our current amplifier) to $\sim 1$ nA. A rich variety of structure is clearly visible in this image plot.

The transition rules listed in Eq. 10 are used to determine the sources of the various features, with $C_\Sigma$, $E_c$ and $\kappa_i$ redefined in Eq. 18-20. All the capacitances are determined beforehand from gate modulation measurements and Eq. 17 in Section 4.1, except for the junction capacitances $C_1$ and $C_2$, which are determined by fitting the slopes of the lines given by Eq. 10 to that of the features in the image. Some important capacitances are $C_1 = 194$ aF, $C_2 = 138$ aF, and $C_{2\text{DEG}} = 335$ aF. $E_c$ is then calculated from the capacitances to be 113 $\mu$eV. The superconducting energy gap $\Delta$ is determined by the minimum threshold from quasiparticle tunneling, which gives $\Delta = 204$ $\mu$eV. The junction resistances are determined from their normal state value.
Figure 25: False color image of $I(V,Q_0)$ surface with 2DEG unconfined. A color table giving the current scale is shown at the top. Transition lines are calculated by the rules in Eq. 10. A contour plot is also added to the positive half of the image.
$R \approx 152 \text{ K}\Omega$, and the Ambegaokar-Baratoff relation then gives $E_J = \frac{h\Delta}{8e^2R} \approx 4 \mu\text{eV}$. As a result, we are in a regime for which $E_J \ll E_C < \Delta$.

The original offset charge $Q_0$ is determined by fitting one of the lines to a corresponding known feature, such as the boundary of the Coulomb blockade for Cooper pair tunneling. The rest of the lines are then calculated using Eq. 10 and the $Q_0$ determined above. The lines are labeled with the initial and final values of $n$ associated with the corresponding transition. The lines with positive slope correspond to tunneling through junction 1, and those with negative slope correspond to tunneling through junction 2.

A contour plot has been added to the positive half of the plot to accentuate the features, with a step of 10 pA from 0 to 500 pA. The lines and features fit very well with each other, indicating the validity of the parameters calculated and the rules used. We can see clearly the three different types of tunneling processes discussed in Section 2.1.2:

- Josephson tunneling, (J-process, dashed lines).

- Quasiparticle tunneling involving pair breaking caused by bias voltage, (e-process, solid lines).

- Quasiparticle tunneling without pair breaking caused by bias voltage, (q-process, dotted lines).

For current to flow through the SET, a cycle of tunneling processes which transfer charge through the two junctions must be completed. A well-known example is the Josephson-quasiparticle (JQP) cycle [20]. It consists of one Cooper pair tunneling through one junction followed by two quaiparticles tunneling through the other, as
Figure 26: Formation of the JQP cycle involving one Cooper pair tunneling from one junction followed by two consecutive quasiparticle tunneling through the other junction.

illustrated in Fig. 26. The cycle can not be completed unless all three of the processes involved are energetically allowed. As a result, the JQP cycle will form a "ridge" along the Josephson tunneling line, which is the resonant condition, and the cycle will not start until bias voltage is above the thresholds for the quasiparticle processes. As we can see from Fig. 25, there is clearly a JQP ridge along the "J: 0 → −2 line when the voltage is above the "e: −1 → 0" line.

Another well-known cycle consists of one Cooper tunneling onto the island through one junction, and immediately tunneling off through the other one, which forms the "supercurrent." No dc voltage is needed for this process, since Cooper pair tunneling is dissipationless. For voltages close to but not equal to zero, some dissipation mechanism such as coupling to the environmental electromagnetic modes or quasiparticle
tunneling must take place to take up the energy difference $eV$.

Besides these well-known features, we also see features associated with the presence of the quasiparticle tunneling without pair breaking, the "anomalous" quasiparticle tunneling process. One example is the Coulomb blockade of this process near zero bias, illustrated as the rhombic region bounded on the right by the "q: $0 \rightarrow -1$" and "q: $0 \rightarrow 1$" lines in Fig. 25. This blockade and the normal Cooper pair blockade (the rhombus in the center bounded on the right by "J: $0 \rightarrow -2$" and "J: $-1 \rightarrow 1$" lines in Fig. 25) combined produce an $e/2$ periodicity for very low bias voltage predicted by van den Brink [21]. Another striking feature are the current peaks along the "e: $1 \rightarrow 0$" in parallel with the JQP peaks at large bias voltages. This anomalous current peak, involving one e-process and q-process through each junction, is not energetically allowed if the anomalous quasiparticle tunneling is not considered.

All these features we see are e-periodic, even the ones at low biases, as shown in Fig. 25. The lack of $2e$ periodicity also indicates the presence of the large quasiparticle tunneling rate, as discussed in Section 2.1.2.

4.3 Characterization of SET with 2DEG Strongly Confined

We repeat the measurement in Section 4.2 when the 2DEG is strongly confined. In this case, the voltages on the gates have been set so that the dot is formed with conductances of the point contacts at about $2G_0$, i.e., the 2DEG is confined into what is referred to as an "open dot".

An image plot of $I(Q_0, V)$ is formed again as discussed above along with the transition lines. This time, we remeasure all the capacitances except $C_1$ and $C_2$, which were determined in the previous measurement. The new charging energy $E_C \approx$
115 \mu eV, and again \( \Delta \approx 204 \mu eV \). The validity of these parameters is once more illustrated by the good agreement between the data and the calculated lines. The image plot is shown in Fig. 27 along with the plot for no 2DEG confinement for purposes of comparison. The same color table is used for both images.

We can see clearly from the two images that although the important energy parameters, such as charging energy \( E_C \) and superconducting gap \( \Delta \) are almost unchanged, there is in general a larger current through the SET when the 2DEG is strongly confined, for both low bias and high bias voltages, while the JQP peak is not as distinct in this case as it was for no confinement.

To take a better look at what happens, we compare the \( I-V \) curves taken for the same value of \( Q_0 \) in the two cases. A typical result of high-bias voltage, intermediate-bias voltage and low-bias voltage for some representative \( Q_0 \) values is shown in Fig. 28.

The results are:

- For high bias voltage, the JQP peak is suppressed when the 2DEG is strongly confined, while the "background" current is strongly increased. This is illustrated in Fig. 28a,b.

- For moderate bias voltage, a much larger current appears when the voltage is above the threshold for anomalous quasiparticle tunneling. This is illustrated in Fig. 28c,d, in which case \( E_c/e \) is the threshold voltage.

- For very low bias voltage, in the supercurrent region, the supercurrent is higher in the strong-confinement case, also with a much higher background. This is illustrated in Fig. 28e,f.
Figure 27: $I(Q_0), V$ surfaces for two different 2DEG confinements. The same color table is used for both images. Transition lines are determined using same values for $C_1$ and $C_2$. 
Figure 28: $I$-$V$ curves for two different 2DEG confinements at representative values of $Q_0$. 
4.4 Changes in the Transport Properties of the SET as the Environment Changes

To have a more complete picture of how the transport properties of the SET change as the environment varies, we perform a series of gate modulation measurements as discussed in Section 3.6.2 for various 2DEG confinements. In these measurements, the left point contact was "completely" pinched-off (with conductance $\sim 0.1G_0$) and both the central gates were activated. The right point contact was gradually pinched off from completely open (conductance $\gg 10G_0$) to nearly closed (conductance of $\sim 1G_0$), at which point charge oscillations began to appear in the 2DEG, i.e., the dot began to form. The average maximum current vs. conductance of the right QPC, and hence the confinement of the 2DEG, is shown in Fig. 29.

The current varies with 2DEG confinement in three different ways for different features:

- For the supercurrent and other low bias features, the current initially rises. As the confinement becomes stronger, it reaches a maximum and begins to decrease. The maximum current for larger biases occurs at higher 2DEG confinements. This is illustrated in Fig. 29a-d.

- For the JQP peak, the current decreases monotonically as the confinement increases. This is illustrated in Fig. 29e.

- For the anomalous quasiparticle peak, the current increases monotonically as the confinement increases. This is illustrated in Fig. 29f.

Similar results can be obtained by decreasing the conductances of both QPCs simultaneously.
Figure 29: Maximum value of $I(Q_0)$ vs. 2DEG confinement at various bias voltages. The vertical dashed line indicates when the dot starts to form in the 2DEG.
4.5 When the 2DEG Becomes a Quantum Dot

We can confine the 2DEG further into the dot regime. Due to beating effects in this double dot system, a complete image plot is difficult to produce, but some important information can still be obtained via the gate modulation measurements using the bottom central gate, as discussed in Section 3.1.

The trends discussed in the previous section extend further into the dot regime: the current oscillations at low bias voltages continue to decrease until they die out, as do oscillations associated with the JQP peak. The anomalous quasiparticle peak, however, increases to some value and remains there, despite the fact that the conductances through the two QPCs become very small due to the electrostatic coupling from the voltage on the gate used to modulate $Q_0$.

4.6 Temperature Dependence Measurement

To be sure that the changes we saw in the transport properties of the SET were not just due to thermal fluctuations, temperature dependence of the transport properties of the SET were tested. We performed gate modulation measurements with the 2DEG grounded at various mixing chamber temperatures from 20 mK to 500 mK to observe the effects of temperature, and compare the results with those observed from the confinement of the 2DEG.

The results can be summarized as follows:

- The temperature of the sample is $< 100$ mK at low bias voltages. This can be seen from Fig. 31, for which the bias voltage was 80 $\mu$V. The shapes of the $I(V_g)$ curve begins to change between $T = 50$ mK and $T = 100$ mK. The trend continues as $T$ is increased past 100 mK.
Figure 30: $I(Q_0)$ vs. voltage on the bottom central gate at various bias voltages after the 2DEG is confined to a quantum dot.
Figure 31: Gate modulation measurements at different temperatures for a bias voltage $V = 80 \mu V$. The curves have been offset from each other in current for clarity.

- Changes in temperature affect the SET differently from changes in 2DEG confinement. This can been seen at both low and the high biases. For example, at $700\mu V$ bias, as shown in Fig. 32, the height of the JQP peak does not change with temperature, even though the background has increased significantly for $T = 500$ mK. This behavior is quite different from the decrease in JQP peak height as the 2DEG is confined.

4.7 Preliminary Explanation

Due to the complexity of the system, especially after the point contacts become quantized, a full explanation of the results will require detailed theoretical work, which is currently underway. In this section, we provide a preliminary qualitative explanation.
Figure 32: Gate modulation measurements at $T = 20$ mK (solid line) and $T = 500$ mK (dotted line) for a bias voltage $V = 700$ $\mu$V. The two curves have been offset from each other in the gate voltage for clarity.

As the impedance of the 2DEG increases, it will give rise to voltage fluctuations at the sample with a spectral density of the Nyquist form [43, 44]

$$S_v(\omega) = \frac{2}{\pi} \frac{\text{Re}Z(\omega)\hbar\omega}{\exp(\hbar\omega/k_BT_{\text{env}}) - 1}$$

(21)

where we treat the 2DEG classically with an impedance $Z(\omega)$.

These fluctuations will result in increased transition rates between states and may introduce the "anomalous" quasiparticle processes via photon assisted tunneling, as discussed in Section 2.1.2. In general, a larger background is expected due to the increased anomalous quasiparticle tunneling rates [44, 45].
On the other hand, dissipation in the environment introduces damping of phase fluctuations in the superconducting junctions which is inversely proportional to the resistance of the electrodynamic environment \([6, 46, 47]\). We therefore expect that when the 2DEG is strongly confined and the environmental impedance presented to the junctions is large, phase fluctuations will not be effectively damped \([16]\), and thus coherent Cooper pair tunneling processes will be suppressed.

The effects of the increased anomalous quasiparticle processes and suppressed Josephson processes will be reflected differently in the current for different bias voltages:

- For the anomalous quasiparticle peak, which requires the anomalous quasiparticle process to complete the cycle but for which no Josephson tunneling is involved, we would expect that the current will become larger as the confinement of the 2DEG increases due to the increase in quasiparticle tunneling rates.

- For the \(JQP\) process, which is initially energetically favorable and does not require anomalous quasiparticle tunneling, suppression of Josephson tunneling leads a decrease in the tunneling rate for this cycle. Hence the height of the \(JQP\) peak decreases as the 2DEG is confined.

- For bias voltages small compared to \(\Delta\), charge transfer takes place via a combination of Cooper and quasiparticle tunneling \([21, 23]\). Competition between an increase in the quasiparticle tunneling rates and a suppression of the Josephson processes results in nonmonotonic behavior of the current. For little or no 2DEG confinement, the quasiparticle tunneling rates are small, and the increase in the quasiparticle tunneling rates aids in the formation of current-carrying cycles and
causes the current to rise. As the quasiparticle tunneling rates increases, the Josephson process is simultaneously suppressed by the increasing 2DEG confinement. Eventually the suppression in the Josephson process rates dominates and the current decreases with the 2DEG confinement.

This qualitative analysis seems to explain many of the experimental results, but a more complete theoretical study is needed and more samples must be tested before a conclusive explanation can be given.
5 CONCLUSIONS AND FUTURE WORK

In this thesis, we have presented experimental studies of the transport properties of an S-SET as the electrodynamic environment is varied. Previous theoretical work have predicted that fluctuations in the environment will cause an increase in quasiparticle tunneling and incoherent Cooper tunneling rates based on models in which the fluctuations are coupled to the SET through the voltage leads. Such impedances are usually small compared to $R_N$, and are difficult to adjust experimentally. Fluctuations in the gates are always neglected in these models.

A novel model system has been devised to study the effects of the environment. The environment is strongly capacitively coupled to the island of the SET and serves as a gate, in which the fluctuations can be large and tunable. An example of such a system consisting of an S-SET coupled to a quantum dot defined by the split gate method on a GaAs/Al$_x$Ga$_{1-x}$As heterostructure has been successfully fabricated. The techniques developed for the fabrication of this sample will be useful in fabricating other samples with similar geometry.

Electrical characterization of the sample has been performed at a mixing chamber temperature of 20 mK. The important energy scales $E_c$ and $\Delta$ are almost unchanged as the confinement of 2DEG varies so that changes in transport are not due to changes in the energetics of the system. Changes in the transport properties of the SET have been successfully observed as the environment varies. Such changes include suppression of Josephson processes, such as the JQP and supercurrent peaks, and enhancement of quasiparticle processes.

A preliminary qualitative explanation has been given to explain these results. A more conclusive explanation requires both further theoretical and experimental work.
Some possible future work includes:

- Fabricate samples with normal metal buffer electrodes on the SET leads as quasiparticle traps [48]. These traps allow the quasiparticle population on the leads to reach the thermal equilibrium value and hence quasiparticles induced through the leads can be neglected. The effects of variations in the 2DEG should thus be more clearly observed in such samples.

- Fabricate samples with smaller junction resistances, in which the supercurrent will be larger so that measurements can be performed more fully into the quantum dot regime.

- Fabricate samples with smaller dots, in which the energy structures are more widely spaced and their effects may be observable via electrical measurements on the SET.

- Another future direction is to fabricate an RF-SET [49], in which a normal state SET, strongly coupled to a dot, is imbedded in an rf circuit. Damping in the circuit is very sensitive to the resistance of SET, which is in turn sensitive to the offset charge of the island. This provides a very fast readout of changes in the offset charge on the SET island. Since the offset charge of the SET is sensitive to dot charge when they are strongly coupled, single electron tunneling on and off the dot may be detected in real time by such a device.
References


