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Modeling and Design of Carbon Nanotube Interconnect for Mixed-Signal VLSI Applications

by

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ABSTRACT

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In future nanoscale integrated circuits, process technology scaling coupled with increasing operating frequencies will exacerbate the resistivity, electromigration, and delay problems that plague interconnect in today's designs. Metallic carbon nanotubes are a promising future replacement for on-chip copper interconnect due to their large conductivity and current carrying capabilities. In this research, we develop modeling and design techniques for carbon nanotube-based interconnect solutions. We create an equivalent RLC circuit model for individual and bundled single-walled and multi-walled carbon nanotubes, which we leverage to determine the optimal design for nanotube-based interconnect solutions. Using the proposed modeling and design techniques, we investigate the performance and reliability of nanotube-based structures in future mixed-signal VLSI applications including digital interconnect and passive components for analog integrated circuits. We also examine the nanotube properties and fabrication requirements necessary for nanotube-based interconnect to be a competitive solution compared to standard copper technology. The results indicate that nanotube-based interconnect solutions will have the potential to revolutionize the next generation of integrated circuits in mixed-signal VLSI applications.
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Chapter 1

Introduction

The tremendous advancement in the field of integrated circuit manufacturing achieved in the past decade can largely be attributed to the successful scaling of CMOS technology. While transistor scaling and increasing operating frequencies have improved overall performance, interconnect for on-chip communication continues to hinder the realization of high performance integrated systems and will ultimately lead to fundamental limits on both performance and reliability [1, 4–12]. As wire width continues to decrease, traditional copper interconnect in high performance VLSI systems will suffer from significant increases in resistivity due to surface roughness and grain boundary scattering [1, 13, 14]. Copper wire scaling will lead to delay problems caused by increased wire resistance and to electromigration problems due to the lower current densities supported by conductors with small cross-sectional areas [1, 15, 16]. Furthermore, the performance and density of on-chip passive components, which play a critical role in analog and mixed-signal VLSI applications [17–21], are also limited by
the material properties of conductors and dielectrics in current VLSI manufacturing process technologies [22-25].

As CMOS technology is pushed to its basic physical limits, alternate technologies are required for the realization of interconnect and on-chip passive components in future high performance mixed-signal integrated circuits. Both single-walled and multi-walled carbon nanotubes (CNT) have been proposed as potential future interconnect solutions due to their large conductivity, small dimensionality, and large current carrying capabilities compared to current scaled copper interconnect technology [16,26-31]. Given the desirable material properties of carbon nanotubes, the modeling, design, and performance/reliability analysis of nanotube-based interconnect solutions for future mixed-signal VLSI applications is a crucial step toward the adoption of this promising technology.

1.1 Thesis Contributions

In this thesis, we develop modeling and design techniques for interconnect based on single-walled carbon nanotubes (SWCNT) and multi-walled carbon nanotubes (MWCNT), which we leverage to investigate the performance and reliability of nanotube-based interconnect solutions for on-chip communication and integrated passive components in future mixed-signal VLSI applications. The research consists of three complementary areas: (1) the modeling of interconnect structures constructed using individual and bundled SWCNTs and MWCNTs; (2) the optimal design and
performance/reliability analysis of nanotube-based interconnect solutions for on-chip communication; and (3) the modeling and design of nanotube-based inductors and capacitors for future mixed-signal VLSI applications. The modeling, design, and performance/reliability analysis of nanotube-based interconnect solutions and passive components presented in this study will help to guide future theoretical and experimental research efforts toward the realization of this promising technology in future high performance nanoscale integrated circuits.

For the scalable modeling of carbon nanotube interconnect structures, we have developed an equivalent RLC circuit model for individual and bundled SWCNTs and MWCNTs [29,32–37]. The model includes a closed-form resistance formulation for SWCNTs and MWCNTs that captures the dependence of the phonon scattering mean free path and of the number of 1-D conduction channels on the nanotube diameter [29,32,35,38,39], which is based on recent experimental observations [2,40–42] and theoretical results [43–46]. Based on the results from the resistance model, we predict that carbon nanotube-based conductors can provide significantly lower resistance than scaled copper interconnect in future integrated circuit fabrication process technologies, particularly for intermediate and global interconnect applications [29,32,38]. The RLC circuit model also leverages a scalable magnetic and kinetic inductance characterization technique for bundles of SWCNTs and MWCNTs based on the partial element equivalent circuit (PEEC) approach [29,32,47,48]. The developed circuit model provides an accurate and computationally efficient means for evaluating the
potential performance and reliability of nanotube-based interconnect solutions for future mixed-signal VLSI applications.

Based on the equivalent RLC circuit model for individual and bundled SWCNTs and MWCNTs, we develop a design technique to determine the optimal nanotube diameter and nanotube bundle dimensions for nanotube-based interconnect in digital VLSI applications [32–34]. Leveraging the aforementioned modeling and design techniques, we evaluate the potential performance advantages of carbon nanotube-based interconnect over scaled copper wires in future process technologies [29,32–34,36,49]. The results indicate that nanotube-based interconnect solutions can provide a significant delay reduction compared to scaled copper wires future process technologies for local, intermediate, and global interconnect applications [29,32–34,36], particularly when the nanotube diameters and bundle dimensions are optimized [32–34]. We also explore the potential reliability implications of statistical variations in SWCNT and MWCNT based interconnect solutions, and in general, we predict that nanotube-based interconnect will most likely experience greater delay variation than scaled copper interconnect due to the variation in nanotube-specific properties. Furthermore, we find that large-diameter MWCNT bundles are significantly more susceptible to process variations than small-diameter SWCNT bundles [32,33,50,51]. Therefore, the impact of statistical process variations must be taken into account during the design and manufacturing processes in order to reliably utilize nanotube-based interconnect solutions in future mixed-signal VLSI applications.
In addition to evaluating the potential performance and reliability of nanotube-based structures for on-chip communication, we also investigate the design and performance of nanotube-based inductors and capacitors, which could have important implications for future analog and wireless integrated circuits and systems [52–55]. Leveraging an extended RLC circuit model that includes the resistive and inductive impact of high frequency current re-distribution, we predict that nanotube-based on-chip inductors could potentially provide significantly larger quality factors than on-chip inductors implemented with standard copper conductors [52,53], which would improve the performance critical analog circuits such as low noise amplifiers (LNA) and RF filters [20–22,56–78]. We also examine the design and performance of several potential nanotube-based capacitor structures and find that nanotube-based capacitors can simultaneously provide significantly greater capacitive densities and quality factors compared to traditional metal and semiconductor based integrated capacitors [54,55]. The results from this study demonstrate that nanotube-based interconnect solutions have the potential to revolutionize the next generation of integrated circuits in mixed-signal VLSI applications if the manufacturing challenges associated with the high density IC-compatible parallel growth of nanotube bundles can be overcome.
1.2 Thesis Organization

The rest of the thesis is organized in the following manner. Chapter 2 discusses the current technology scaling problems associated with standard copper interconnect technology and possible alternative technologies, the physical and electrical properties of carbon nanotubes, and previous experimental and theoretical research related to carbon nanotube-based interconnect. In Chapter 3, we develop an RLC circuit model for individual and bundled SWCNT and MWCNTs. Chapter 4 investigates and compares the resistance of CNT and copper-based interconnect solutions. In Chapter 5, we create an optimal design technique for nanotube-based interconnect solutions and compare their performance to that of standard copper technology. Chapter 6 discusses the reliability implications of process variations for carbon nanotube interconnect. Chapters 7 and 8 presents the modeling, design, and performance analysis of integrated inductors and capacitors constructed using carbon nanotubes. Chapter 9 summarizes the key contributions of this thesis and presents possible future research directions.
Chapter 2

Carbon Nanotube Interconnect

The impact of interconnect on performance and reliability continues to increase as process technology scales downward. In the future, process technology scaling coupled with increasing operating frequencies will exacerbate the delay, noise and power problems that already plague interconnect in today’s designs [1,4–12]. Traditional interconnect materials will suffer from electromigration and electromagnetic interference problems due to technology scaling [1,15,16,79–81]. Furthermore, as wire widths continue to decrease, copper interconnect will suffer from significant increases in resistivity due to surface roughness and grain boundary scattering [13,14]. Figure 2.1 displays the resistivity of copper interconnect versus wire width predicted the 2005 International Technology Roadmap for Semiconductors (ITRS) [1]. For local interconnect with a 22 nm wire width (22 nm process technology), the wire resistivity is approximately 300% larger than the resistivity of bulk copper. As process technology scales beyond the 22 nm node, copper wire resistivity rapidly increases, which lim-
its the performance and current carrying capabilities of on-chip copper interconnect. While interconnect has greatly benefited from recent advances in technology such as the transition from aluminum to copper wires and the introduction of low-k interconductor dielectrics [82], these solutions only provide one-time benefits. Therefore, future interconnect solutions will require more radical alternatives.

2.1 Future Potential Interconnect Solutions

To alleviate the problems associated with copper interconnect in current and future VLSI applications, several alternative technologies have been proposed. Three-dimensional integrated circuits have the potential to relieve the projected problems with both copper interconnect and mixed-signal system-on-chip (SoC) integration. By distributing components across multiple device layers, average interconnect length will
be substantially reduced, thereby reducing the power and delay requirements imposed by global interconnect [4,9,79,83–86]. While the thermal and manufacturing problems associated with 3-D interconnect solutions are currently being addressed [83,84], 3-D interconnect still relies on copper conductors that will experience the same resistivity and electromigration issues facing standard 2-D copper interconnect solutions as wire dimensions scale downward [13–16].

With wireless/RF interconnect, global data and clock signals are transmitted across the entire chip using RF mediums, which could increase bandwidth, decrease delay, and reduce the dependence on standard copper interconnect for global on-chip communication [87,88]. However, the size and complexity of integrated transceivers coupled with substantial electromagnetic interference issues currently limit the feasibility of wireless/RF interconnect [8]. Optical interconnect offers the promise of increased bandwidth, decreased delays, lowered power consumption, and reduced electromagnetic interference [89], but several challenges such as subwavelength optical confinement [90–95] and the efficient design and implementation of modulators, detectors, and transimpedance amplifiers are still open research questions that need to be addressed [15,96]. Given the challenges facing these interconnect solutions, other technologies such as carbon nanotubes must also be considered for on-chip communication and passive components in future VLSI applications.
2.2 Carbon Nanotube-Based Interconnect

Both SWCNTs and MWCNTs have been proposed as possible replacements for on-chip copper interconnect due to their large conductivity, small dimensionality, and large current carrying capabilities [16, 26–30]. SWCNTs are rolled graphitic sheets that can either exhibit metallic or semiconducting behavior depending on their chiral vector, which measures the direction in which the SWCNT is rolled with respect to the underlying graphene lattice (chirality) [97]. SWCNTs with diameters ranging from 0.4 nm to 4 nm have been realized [41, 98]. With reported current densities on the order of $10^9 \text{A/cm}^2$, SWCNTs have significantly larger current carrying capabilities than traditional metallic interconnects, which typically have current densities on the order of $10^5 \text{A/cm}^2$ [16, 30]. Therefore, due to their covalently bonded structure, carbon nanotubes are extremely resistant to electromigration [30]. In addition, SWCNTs can have significantly lower resistivity than scaled copper interconnect. In [99], a resistance of approximately $4 \text{k} \Omega/\mu\text{m}$ was reported for a metallic SWCNT with a diameter of 1.8 nm. This results in a resistivity of approximately $1.0 \mu\Omega\cdot\text{cm}$, which is a 44% reduction from the resistivity of bulk copper ($1.8 \mu\Omega\cdot\text{cm}$) and a 77% reduction from the resistivity of copper interconnect with a 22 nm width predicted by [1] ($4.4 \mu\Omega\cdot\text{cm}$).

MWCNTs are also a potential solution for on-chip interconnect applications. MWCNTs consist of several rolled graphitic shells nested inside each other and can have diameters as large as 100 nm [2, 40, 100]. Until recently, experimental results
indicated that current only flows through the outer shell in MWCNTs, which places a lower limit on their resistivity [101–103]. However, recent experimental research has demonstrated that it is possible to contact the interior shells in a MWCNT structure, which leads to significantly lower resistivity [2, 40, 104, 105]. Since MWCNTs are significantly larger than their single-walled counterparts, individually they have less total resistance than an individual SWCNT and have been shown to have resistivity values on the same order as SWCNTs [40, 106]. For instance, in [40] a 25 μm long MWCNT with a diameter of 100 nm had a measured resistance of 34.4 Ω, which results in a resistivity of approximately 1.1 μm-cm. MWCNTs have also exhibited similar current carrying capabilities to SWCNTs [105].

While individual SWCNTs and MWCNTs have desirable material properties, they suffer from a large intrinsic resistance that is not dependent on the length of the nanotube [31, 40, 107]. Therefore, individual CNTs cannot be used alone in many VLSI applications to construct high performance interconnect. To alleviate this intrinsic resistance problem, bundles or ropes of CNTs in parallel have been proposed and physically demonstrated as a possible interconnect medium [27, 28, 108]. SWCNT bundles have metallic nanotubes that are randomly distributed within the bundle. With no special separation techniques, the metallic nanotubes are distributed with probability 1/3 since one-third of possible SWCNT chiralities are metallic [97]. However, significant research efforts are underway to develop techniques to separate metallic and semiconducting SWCNTs [109–113]. For MWCNTs, the nested shells also have ran-
Figure 2.2: Nanotube bundle-based interconnect constructed of large diameter MWCNTs, small diameter MWCNTs, or SWCNTs.

dom chiralities with a 1/3 probability of being metallic. The statistical distribution of metallic nanotubes can have important reliability and performance implications for nanotube bundle-based interconnect and passive components as we discuss in Chapter 6.

Based on the previously described physical and electrical characteristics of CNTs, we consider nanotube bundle-based interconnect constructed using SWCNTs and MWCNTs in this study. We envision three possible nanotube-based interconnect structures: SWCNT bundles, small diameter MWCNT bundles, and individual or bundled large diameter MWCNTs. These three configurations are depicted in Figure 2.2. Unless otherwise specified, we assume that all of the CNTs in the bundle are contacted on both ends with metal electrodes, which provide connectivity to other
interconnect segments and devices in VLSI systems [3]. The metal electrodes are typically constructed using metals such as gold, palladium, aluminum, or titanium [114]. The spacing between the CNTs in the bundle can range from approximately 0.3 nm, which is due to the van der Waals forces between the CNTs, to 10s of nanometers depending on the synthesis technique used to create and position the nanotubes in the bundle [3,108]. We discuss the possible CMOS-compatible fabrication solutions that are currently being developed for the aforementioned CNT-based interconnect structures in more detail in the following sections.

### 2.3 Synthesis of CNT Structures for Interconnect

For CNT bundles to be an attractive interconnect solution, CNT-based interconnect must not only reliably achieve greater performance than scaled copper interconnect but also must have a cost-effective means of fabrication in future nano-scale integrated circuits (IC). In general, there are three leading synthesis techniques for carbon nanotubes: (1) arc discharge; (2) laser ablation; and (3) chemical vapor deposition (CVD). In arc discharge methods, a large voltage is applied between two graphite rods, which may be doped with a metal catalyst, in an inert gas environment. The large voltage causes an electric arc to form between the electrodes, which generates either SWCNTs or MWCNTs depending on the catalyst material and inert gas utilized [115–117]. While arc discharge provides a relatively inexpensive means for generating CNTs, the purity of the synthesized CNTs is relatively low [116]. Laser ablation
methods are similar to arc discharge except they utilize a high power laser aimed at a graphitic source to generate the SWCNTs and MWCNTs [108,116,118]. Laser ablation typically produces CNTs with fewer defects compared to arc discharge [108,116]. Note that in most cases when CNTs are synthesized using arc discharge or laser ablation, the synthesis process typically forms CNT bundles where the individual CNT diameters are highly correlated [108,116,119–121].

Arc discharge and laser ablation have several drawbacks that currently limit their utilization for the large-scale fabrication of nanotube-based interconnect solutions. CNTs generated using arc discharge and laser ablation must be purified to remove unwanted amorphous and graphitic carbon [26,116]. Furthermore, temperatures exceeding 1000 °C are required to generate CNTs with low numbers of defects [26,116], which is significantly greater than the 450 °C limit imposed by the low-k material used for interconnect dielectrics [2]. Furthermore, arc discharge and laser ablation do not currently provide a mechanism for the large-scale IC compatible placement of CNTs for interconnect applications [26] unless complex processing steps such as dielectrophoresis are used [109,110,122].

Recently developed chemical vapor deposition (CVD) based techniques for synthesizing multiple nanotube bundles in parallel have demonstrated potential as a cost-effective and CMOS-compatible solution for fabricating CNT bundles for interconnect applications [2,3,26,123,124]. The diameter of the nanotubes in bundles generated using this approach can be controlled based on the metallic catalyst par-
ticle size, and the nanotube-bundle dimensions can be lithographically defined by depositing catalyst metal in locations where the interconnect is to be placed. One of the major limitations currently facing CVD-based nanotube bundle fabrication techniques is the relatively low density of nanotubes, which decreases the resistance of the bundle. In [3], vertically aligned MWCNTs with approximately 5 nm diameters were fabricated using a CVD-based process at 450 °C, and a nanotube density of $10^{12}$ nanotubes/cm$^2$ was achieved, which provides a CNT area coverage in the bundle of approximately 20% and an average spacing between the CNTs in the bundle of approximately 6 nm, which is significantly larger than the 0.3 nm spacing in CNT bundles due to van der Waals forces alone [108]. Horizontally aligned nanotubes were realized with even lower density [3]. However, recent research has demonstrated that it is possible to attain a 19x to 25x improvement in CNT density by immersing the CNT bundles in an organic solvent after the nanotube bundles are synthesized using the CVD process [125,126]. We further describe recent research efforts aimed at integrating CNT-based interconnect in future nano-scale integrated circuits using CVD-based synthesis methods in Section 2.4. Consequently, CVD-based synthesis methods are currently the most promising approach for the large-scale and cost-effective IC compatible fabrication of nanotube-based interconnect solutions in future process technologies.
2.4 Experimental Electrical Characterization and Fabrication of CNT Interconnect

Over the past decade, substantial research efforts have been dedicated to the electrical measurement of carbon nanotubes. Numerous studies have investigated the resistance [16,31,42,99,107,127–135] and high frequency electrical characteristics [136–141] of individual and bundled SWCNTs and the resistance [40,103–105,142–151] and high frequency electrical characteristics [152–156] of individual and bundled MWCNTs. We discuss the key results from these experimental studies in more detail where applicable when we develop an equivalent RLC circuit model for nanotube-based interconnect in Chapter 3.

In addition to research studying the electrical characteristics of carbon nanotubes in general, several experimental investigations targeting the electrical measurement and IC compatible fabrication of potential nanotube-based interconnect structures have recently been performed [2,3,27,28,114,157–162]. Initial experimental efforts were targeted toward the realization of CNT-based vertical interconnects for vias between horizontal metal layers in VLSI applications [2,3,27,28,157,158,163] since the vertical growth of CNTs on a planar surface is substantially easier to accomplish than horizontal CNT growth using CVD-based fabrication methods [3,26]. The fabrication of vertical CNT-based interconnect structures has been accomplished using two different techniques: a bottom-up approach [27,158] and a buried catalyst approach [2,3,28,157,163]. In the bottom-up approach, the CNT-based via positions
are first defined by lithography patterning catalyst layers such as Ni [27] or a combination of $Al_2O_3$ and Fe [158]. The CNT bundles are then grown vertically using CVD with an electric field applied normal to the substrate in order to vertically align the CNTs in the bundle. For interconnect applications, $SiO_2$ is then deposited in the region surrounding the CNT-based vias and metal electrodes are deposited on top of the CNT-based via [27].

In the buried catalyst approach for fabricating vertical CNT-based interconnects, a blanket deposition of a catalyst layer of Ni, Co, or Fe is performed followed by a blanket deposition of a layer of $SiO_2$, which forms the dielectric layer between metal layers [28,157,163]. To better control the diameter of the CNTs in the bundles that form the vias, size-controlled catalytic metal nano-particles may be deposited on the substrate instead of the blanket catalyst layer [2,3]. The $SiO_2$ is then selectively etched down to the catalyst material where the CNT-based vias are to be placed. A CVD process is then utilized to grow the CNT-based via in the etched trenches where the catalyst material is exposed. Once the CNTs have grown to a sufficient length to complete the electrical connection between metal layers, metal electrodes are deposited on top of the CNT-based via [2,3,28,157,163]. A similar approach has been utilized to fabricate CNT-based via holes between device layers for 3-D interconnect applications [159].

In general, vias constructed using the bottom-up and buried catalyst approaches have been realized using MWCNT bundles [2,3,27,28,157,158,163]. SWCNT bundles
are difficult to generate using these methods since they require small metal catalyst particles that have the tendency to coalesce into large particles during the CVD growth process [2, 3]. To date, the lowest resistivity attained by a fabricated CNT bundle-based via is 530 μm·cm, which is 2 orders of magnitude larger than the resistivity of scaled copper wires used in current interconnect applications [2, 3]. However, the resistivity of the realized vias is rapidly decreasing with improvements in the CVD-based fabrication process, with decreases in the CNT diameter, and with increases in CNT density [3]. Densification techniques for CNT-bundles also have the potential to decrease the resistivity of CNT-based vias by an order of magnitude or more [125, 126].

In addition to exploring the electrical performance and fabrication of CNT-based vias, recent research has also begun to investigate the realization of horizontal nanotube-based interconnect. In [160], researchers at Intel performed high frequency electrical measurements up to 50 GHz on a SWCNT bundle fabricated on a silicon wafer using a CVD process. The results indicated that the large predicted kinetic inductance for an individual SWCNT will only have a small impact on the performance of SWCNT bundle-based interconnect, which experimentally confirms our previous theoretical predictions in [49]. Researchers at Toshiba and Stanford have recently combined MWCNT bundle-based interconnect with CMOS transistors and performed electrical measurements at frequencies up to 15 GHz [114, 161, 162]. The MWCNT bundle interconnect was combined with the CMOS test chip post-fabrication using dielec-
trophoresis to position MWCNTs between two gold electrodes deposited on top of the test chip. The gold electrodes were then connected to the test chip using titanium vias [161]. The interconnect enabled the 1 GHz operation of ring oscillators connected through the CNT-based interconnect, which is the fastest hybrid CMOS-CNT interconnect circuit constructed to date [161]. The aforementioned experimental research demonstrates the potential performance advantages and IC compatible growth of CNT-based interconnect solutions in future mixed-signal VLSI applications.

2.5 Modeling and Design of CNT Interconnect

The experimental research on carbon nanotube interconnect described in the previous sections has coincided with the development of theoretical electrical models and design techniques for carbon nanotube interconnect solutions over the past several years. Initial modeling efforts for CNT-based interconnect focused on the development of RLC circuit models for individual and bundled SWCNTs. Burke introduced the first RLC model for an individual SWCNT that models the nanotube as a 1-D quantum wire with a quantum capacitance, kinetic inductance, and a perfect contact resistance between the nanotube and its metal contacts. The model also captures the electrostatic capacitance and magnetic inductance of the nanotube to form an equivalent transmission line model [164,165]. Salahuddin, Lundstrom, and Datta also explored the electronic transport properties in 1-D quantum wires such as individual SWCNTs and produced similar results to Burke's models [166].
Based on Burke's model, Raychowdhury and Roy developed an RLC model for SWCNT bundles that included the additional per unit length resistance due to acoustic-phonon scattering and the resistive increases due to optical phonon scattering when high bias voltages are applied [167]. Also leveraging Burke's model, Srivastava and Banerjee analyzed the impact of imperfect metal-nanotube contacts and discussed the increase in overall resistance when some of the nanotubes in the bundle are semiconducting [168]. Naeemi and Meindl proposed a mono-layer SWCNT structure for local interconnect and demonstrated that the high bias resistance due to optical phonon scattering will not have a large effect for most predicted interconnect geometries [169–171]. They also examined the performance of SWCNT bundle-based interconnect in the context of local and global interconnect and concluded that SWCNT bundles can provide superior delay to copper interconnect in future process technologies [172]. Atomic-level simulations by Zhou, Sreekala, Ajayan and Nayak have also confirmed that SWCNT bundles can provide lower resistance than copper interconnect for wire dimensions less than 60 nm [173]. For integrated passive components in VLSI applications, SWCNT bundle-based capacitors were examined in [174] and shown to have significantly larger capacitive density than capacitors implemented in standard CMOS technology.

Given the reported promising experimental resistance results for end-contacted MWCNTs [40], electrical models and design techniques have also recently been investigated for MWCNT-based interconnect solutions. Naeemi and Meindl have ex-
examined the resistance of MWCNTs and developed qualitative design guidelines for interconnect constructed using bundles of MWCNTs [106,175]. They concluded that SWCNTs generally will provide less delay than MWCNTs for local interconnect applications, but MWCNTs will have less delay for global interconnect [175]. Mao et al. have also recently investigated the modeling and performance of MWCNT bundle-based interconnect [176] and provided similar design guidelines to the ones proposed in [175]. Wang et al. examined the resistance and inductance of CNT bundles consisting of both MWCNT and SWCNT [177,178] and obtained similar results to previous studies on SWCNT/MWCNT resistance and SWCNT inductance [38,47,106].

Over the past several years, we have also contributed to the modeling and design of SWCNT and MWCNT-based interconnect solutions and their applications to both on-chip communication and passive components in mixed-signal VLSI systems [29,32–39,47–55,179–181]. In [38,39], we developed a diameter-dependent resistance model for SWCNT bundles that captures the diameter dependence of individual SWCNT ohmic and contact resistances and their impact on the overall bundle resistance based on recent experimental observations [41,42] and theoretical results [43–46]. We also developed a scalable model for the magnetic and kinetic inductances of SWCNT bundles [47–49]. Leveraging our resistance and inductance models, we created an equivalent RLC circuit mode for SWCNT bundles, which we utilized to explore the potential performance advantages of SWCNT bundle-based interconnect [29,36,37,179,180] and on-chip inductors utilizing SWCNTs [52,53]. We
also explored the potential reliability implications of statistical variations of SWCNT and MWCNT physical properties for nanotube-based interconnect [32,33,50,51]. Recently, we have expanded our circuit model for SWCNT bundles to model MWCNT bundles, and based on this model, we have developed quantitative design techniques for generalized CNT-based interconnect consisting of both SWCNTs and MWCNTs, which we leverage to predict the performance and fabrication requirements for future CNT-based interconnect solutions [32-34]. We have also examined the design and potential performance benefits provided by MWCNT-based capacitors for mixed-signal VLSI circuits [54,55]. In the remaining chapters of this thesis, we provide a holistic explication of our research on the modeling and design of CNT-based interconnect solutions for mixed-signal VLSI applications.
Chapter 3

Modeling of Carbon Nanotube Interconnect

To understand the performance and reliability implications of carbon nanotube-based interconnect for future mixed-signal VLSI applications, scalable circuit models must be developed to accurately capture the electrical characteristics of CNT-based interconnect solutions. Atomic-level simulations provide the greatest level of accuracy, but an intractable amount of CPU time is required for the simulation of realistic interconnect geometries (months of CPU time on a teraflop supercomputer reported in [173] for a single SWCNT bundle). Given the increasing complexity of interconnect in current and future nano-scale integrated circuits, circuit models based on analytical resistance, capacitance, and inductance formulations are needed to characterize the performance and reliability of nanotube-based interconnect. RLC circuit
models have the added advantage of being able to leverage existing simulation tools, well-established circuit theory, and numerical modeling and model order reduction techniques that are currently utilized for the efficient modeling and design of copper interconnect in current VLSI systems [81,182–198]. In this chapter, we develop an equivalent RLC circuit model for individual and bundled SWCNTs and MWCNTs for interconnect applications leveraging recent experimental measurements and theoretical results for electronic transport in CNTs.

3.1 Circuit Model for CNT Bundle Interconnect

To predict the performance characteristics of CNT bundle-based interconnect in future process technologies, we have developed a generalized circuit model for coupled CNTs, which is displayed in Figure 3.1. Note that the circuit model treats an SWCNT as an MWCNT with a single graphitic shell without the loss of generality. For the circuit elements that exist for each shell in the MWCNT, the index $i$ is used in Figure 3.1 to delineate between the circuit elements. Two subscripts $i$ and $j$ are used to delineate between the circuit elements that couple between two MWCNT shells. For MWCNTs, the model assumes that all of the graphitic shells are connected to the metallic contacts as reported in [2,40,100,104].

The model captures both DC conductance and high frequency impedance due to capacitive and inductive effects for each graphitic shell in general CNT bundle-based interconnect geometries consisting of large diameter MWCNTs, small diameter
Lumped Distributed Lumped


circuit for coupled CNTs. Note that the circuit model treats an SWCNT as an MWCNT with a single conducting shell without the loss of generality.

Figure 3.2: Equivalent circuit model for two coupled CNT bundle interconnect wires.

MWCNTs, or SWCNTs, which are depicted in Figure 2.2. The model is based on the Luttinger liquid formalism for 1-D conductors that is employed to model individ-
ual SWCNTs in [164, 165]. To reduce the complexity of the performance analysis of CNT-based interconnect in VLSI applications, the full RLC circuit model displayed in Figure 3.1 can be simplified into the aggregated equivalent circuit model for two coupled CNT bundle interconnect wires displayed in Figure 3.2. In the following sections, we describe the physical origin of each element in the two equivalent RLC models displayed in Figure 3.1 and 3.2 and the modeling techniques utilized to calculate the circuit element values.

3.2 Resistance Modeling

The resistance of an individual graphitic shell of an MWCNT or an individual SWCNT includes an intrinsic quantum ballistic resistance \( R_i \), a lumped contact resistance \( R_c \) due to imperfect metal-nanotube contacts, a distributed ohmic resistance \( R_0 \) due to acoustic phonon scattering, and a high bias resistance \( R_{hb} \) due to optical phonon scattering [31,99,107]. For MWCNTs, an inter-shell tunneling resistance \( R_{tun} \) exists between adjacent shells [103,199]. For both SWCNTs and the outer shells of MWCNTs, an inter-tube tunneling resistance \( R_t \) also exists [133,199].

The ballistic, contact, ohmic, high bias, and tunneling resistances depend on the number of 1-D conduction channels \( N_c \) associated with each shell. For metallic SWCNTs and small diameter metallic MWCNT shells, \( N_c = 2 \), since 2 sub-bands cross the Fermi level. \( N_c \approx 0 \) for semiconducting SWCNTs and small diameter semiconducting MWCNT shells. As the diameter of the conducting shells in the
MWCNT increases, $N_c$ for each shell increases due to the increasing number of sub-bands that play a role in conduction, and this increase occurs in both the metallic and semiconducting shells [40]. To obtain the $N_c$ value for the metallic and semiconducting graphitic shells in large diameter MWCNTs, we use the formulation [106]

$$N_c = ad_s + b$$

(3.1)

where $d_s$ is the diameter of a given MWCNT shell. The constants $a$ and $b$ are determined based on the data presented in [106].

### 3.2.1 Intrinsic and Contact Resistance

For a given conducting shell in an MWCNT or in an individual SWCNT, the intrinsic resistance is

$$R_i = \frac{R_q}{N_c}.$$  

(3.2)

$R_q$ is the basic quanta of conductance for a conduction channel in a 1-D quantum wire,

$$R_q = \frac{h}{2e^2} \approx 12.9 \ k\Omega$$

(3.3)

where $h$ is Planck's constant and $e$ is the charge of a single electron [31]. Regardless of its length, an MWCNT shell or an SWCNT will have a minimum resistance of $R_i$.

$R_c$ models the increased lumped resistance due to imperfect metal contacts. As nanotube fabrication and bonding techniques have been improved, the additional
resistance due to imperfect contacts has been significantly reduced and in several experimental cases has approached 0 (i.e. $R_i + R_c = R_i$) [31,132,200]. However, recent experimental and theoretical results have revealed that the contact resistance of a SWCNT greatly increases when the diameter of the SWCNT ($d_t$) is less than 2.0 nm [42,43]. Based on the experimental data obtained in [42] for Palladium and Rhodium contacts, the normalized increase in contact resistance ($D_{rc}$) due to the decrease in nanotube diameter can be fit to a quadratic rational function. Note that the empirical expression for $D_{rc}$ should be modified based on experimental data for different fabrication techniques, contact materials, and contact bonding configurations.

Therefore, we model the overall contact resistance using

$$R_c = D_{rc}R_{cnom} \text{ if } d_t < 2.0 \text{ nm} \quad (3.4)$$

$$R_c = R_{cnom} \text{ if } d_t \geq 2.0 \text{ nm}. \quad (3.5)$$

As a result, SWCNTs with small diameters can experience significant increases in contact resistance. For large diameter MWCNTs, the lumped contact resistance for a given conducting shell is

$$R_c = 2R_{cnom}/N_c. \quad (3.6)$$

The value of $R_{cnom}$ is highly dependent on the fabrication process utilized to create the CNT-based interconnect structure, which is still an active area of research [3].
3.2.2 Ohmic and High Bias Resistance

When low bias voltages are applied to the CNT ($V_b \leq \approx 0.1V$), the per unit length resistance due to acoustic phonon scattering ($R_o$) is

$$R_o = \frac{R_0 L}{N_c \lambda_{ap}}. \quad (3.7)$$

where $L$ is the length of the nanotube and $\lambda_{ap}$ is the mean free path of acoustic-phonon scattering [31]. Recent experimental evidence and theoretical formulations have demonstrated that $\lambda_{ap}$ depends on the diameter of the CNT for both metallic and semiconducting SWCNTs and MWCNT shells [41,44-46]. The resistance of an individual graphitic shell versus diameter is governed by

$$R_o = \frac{h\alpha LT}{2e^2v_F d_s N_c} \quad (3.8)$$

where $v_F$ is the Fermi velocity in graphene, $v_F = 800,000m/s$, $T$ is the temperature in Kelvin, and $\alpha$ is the total scattering rate of the CNT [41,44]. For metallic and semiconducting nanotubes, (3.8) is valid across a broad range of temperatures [44,45]. Using atomic force microscopy, the electronic mean free path of a metallic SWCNT with a diameter of 1.8 $nm$ was experimentally measured to be approximately 1.6 $\mu m$ in [99]. Using this experimental measurement for $\lambda_{ap}$ and the diameter-dependent expression for $R_o$, we calculate the diameter-dependent equivalent ohmic resistance
of an MWCNT shell or an individual SWCNT using

\[ R_o = \frac{R_d L}{N_c d_s C_\lambda} \]  

(3.9)

where \( C_\lambda \) is a mean free path-to-nanotube diameter proportionality constant defined as

\[ C_\lambda = \frac{\lambda_{ap}}{d_s} \approx \frac{1600 \text{ nm}}{1.8 \text{ nm}} \approx 888.9 \]  

(3.10)

based on the experimental data obtained in [99]. As nanotube fabrication techniques improve, the mean free path should increase thereby enlarging \( C_\lambda \).

When high bias voltages are applied to the CNT (\( V_b \approx 0.1 V \)), the MWCNT shells or individual SWCNTs have an additional high bias resistance \( (R_{hb}) \) due to high energy optical phonon scattering,

\[ R_{hb} = \frac{V_b}{I_o} \frac{2}{N_c}, \]  

(3.11)

where \( I_o \) is the saturation current for a small diameter MWCNT shell or an individual SWCNT [105,107]. For MWCNTs or individual SWCNTs with diameters greater than 2 nm, \( I_o \) is approximately 20 to 25 \( \mu A \) [105,107]. For SWCNTs with diameters smaller than 2 nm, \( I_o \) substantially decreases to a value of approximately 5 \( \mu A \) when the SWCNT diameter is reduced to 1 nm [42]. While high bias voltages can significantly increase the resistance of CNT bundles, the worst case analysis presented in [171] suggests that the maximum voltage drop does not greatly impact the resistance unless
the number of nanotubes in a bundle is small \((N_b < 50)\) and the length is small \((L < 10\lambda_{op})\). Therefore, \(R_{hb}\) has been shown to have a relatively small impact on delay for the nanotube bundle geometries utilized in most interconnect applications [171].

3.2.3 Inter-Shell and Inter-Tube Resistance

Both an inter-shell tunneling resistance \((R_{tun})\) between adjacent MWCNT shells and an inter-tube resistance \((R_t)\) between adjacent CNTs also exist and are captured in the detailed circuit model depicted in Figure 3.1. For most interconnect applications where the same bias voltage is applied to each conducting shell of each nanotube in the bundle, the impact of \(R_{tun}\) and \(R_t\) will typically be relatively small since the per unit length voltage drop across adjacent nanotubes shells will be approximately equal. However, for certain applications such as CNT-based capacitors (Chapter 8) or nanotube bundles with some of the individual CNTs not connected to the external metallic contacts (Section 4.3), \(R_{tun}\) and \(R_t\) can potentially have a significant impact on performance.

We calculate the inter-shell tunneling resistance between adjacent shells based on the results from the tight-binding model presented in [199] for MWCNTs with defects. For two adjacent MWCNT shells, the per unit length inter-shell tunneling resistance is calculated using

\[
R_{tun} = R_q \left( \frac{4}{I_s N_{ds}} \right) \left( \frac{1}{N_c^2} \right) \left( \frac{D_o}{d_s} \right)^2 \left( \frac{L_{o1}}{L} \right) \tag{3.12}
\]
where $I_s$ is a constant that is proportional to the inter-shell conductance, $n_{ds}$ is the number of defects per unit length for a given MWCNT shell, $d_s$ is the average diameter of the adjacent MWCNT shells being considered, and $D_o$ and $L_{o1}$ are diameter and length proportionality constants based on experimental measurements [199]. Based on the experimental inter-shell resistance ($R_{tun} \approx 10k\Omega/\mu m$), nanotube diameter ($D_o \approx 17 \text{ nm}$), and nanotube length ($L_{o1} \approx 1 \mu m$) measured in [103], $4/(I_s n_{ds}) \approx 4.61$ assuming that $N_c$ is 2.4 based on [106] for a metallic shell with a diameter of 17 nm.

We calculate the inter-tube resistance ($R_t$) between two CNTs based on their tunneling barrier resistance [133],

$$R_t = \frac{R_q L_{o2}}{2} e^{2k(S_t + d_t)},$$

where $S_t$ is the edge-to-edge spacing between nanotubes in the bundle, and $k$ and $L_{o2}$ are determined based on experimental measurements. Assuming the 2 $M\Omega$ inter-tube coupling resistance measured in [133] for an experimental nanotube length ($L_{o2}$) of 200 nm, an inter-tube distance of 0.34 nm, and a SWCNT diameter of 1.4 nm, we assume that $k \approx 1.65 \text{ nm}^{-1}$ in this study.

### 3.2.4 Resistance for Aggregate CNT Bundle Circuit Model

Based on the ballistic, contact, ohmic, and high bias resistances for MWCNT shells or individual SWCNTs, we calculate the aggregate resistances utilized in the equivalent circuit model for two coupled CNT bundle interconnect wires displayed
in Figure 3.2. For the ballistic, contact, ohmic, and high bias resistances, the total bundle resistance is the parallel combination of the resistances for each nanotube. For instance, the total intrinsic resistance for a nanotube bundle \((R_{ib})\) is

\[
R_{ib} = \frac{1}{G_{ib}}, \quad G_{ib} = N_b \sum_{j=1}^{N_s} R_{ij}
\]  

(3.14)

where \(R_{ij}\) is calculated based on (3.2), \(N_b\) is the number of CNTs in the bundle, \(N_s\) is the number of graphitic shells in an individual CNT, and the index \(j\) refers to the shell number in the circuit model depicted in Figure 3.1. The total contact, ohmic, and high bias resistances for the nanotube bundle, \(R_{cb}, R_{ob},\) and \(R_{hbb}\), respectively, are calculated in the same manner as (3.14).

### 3.2.5 Total CNT Bundle Resistance

For the design of CNT-based interconnect and passive components, the total resistance of the nanotube bundle including the ballistic, contact, ohmic, and high bias resistances is an important design parameter as discussed in Chapters 5 and 7. The total resistance of a CNT \((R_{tot})\) is given by the parallel combination the resistances of its individual conducting shells,

\[
R_{tot} = \frac{1}{G_{tot}}, \quad G_{tot} = \sum_{j=0}^{N} \left( \frac{1}{R_{jL}} \frac{1}{C_{r}(d_{in}+jS_{n})N_c + \frac{R_{f}}{N_c}} \right),
\]  

(3.15)
where \( d_{in} \) is the diameter of the innermost shell of the CNT, and \( S_s \) is the center-to-center spacing between the adjacent shells in the MWCNT and is typically assumed to be 0.68 nm (0.34 nm shell thickness and 0.34 nm shell-to-shell spacing) [40]. \( R_f \) is the lumped resistance associated with a CNT shell when \( N_c = 2 \), which is given by
\[
R_f = (R_i + R_c + R_{hb})
\]
where \( R_i \), \( R_c \), and \( R_{hb} \) are defined in (3.2), (3.6), and (3.11), respectively. Note that the first term in the denominator of the summation in (3.15) is the acoustic-phonon scattering resistance for each shell defined in (3.9). The number conducting shells in the CNT \( (N_s) \) is \( N + 1 \) with
\[
N = \frac{(d_{out} - d_{in})}{S_s}
\]
where \( d_{out} \) is the outer diameter of the CNT.

When modeling individual or bundled MWCNTs and SWCNTs throughout this paper, we use the average \( N_c \) value for the metallic and semiconducting shells in a given MWCNT or the average \( N_c \) value for the metallic and semiconducting SWCNTs in an SWCNT bundle. For an SWCNT bundle or for the small diameter shells in an individual or bundled MWCNT, we assume that \( N_c = 2P_m \) where \( P_m \) is the probability that a given graphitic shell has a metallic chirality. To obtain the average \( N_c \) value for the metallic and semiconducting graphitic shells in large diameter MWCNTs in (3.15), we use the formulation
\[
N_c = a(d_{in} + jS_s) + b
\]
where \( a \) and \( b \) are the constants defined in [106] for \( P_m = 1/3 \). Note that the constants \( a \) and \( b \) can be modified to model other possible \( P_m \) values for the large diameter shells of MWCNTs, but in practice, increasing \( P_m \) beyond 1/3 for the graphitic shells in MWCNTs is extremely difficult [201].
To develop a closed-form formulation for $R_{tot}$, we expand the summation in (3.15), and after extensive algebraic manipulation, we arrive at the following expression for the total resistance of a large diameter MWCNT:

$$R_{tl} = \frac{-2C_f^2R_f^3S_s}{A_1A_2 + A_3(D_1 - D_2)}$$

(3.16)

where

$$A_1 = 2bC_{\lambda}R_f + a(C_{\lambda}(d_{in} + d_{out})R_f - 2R_qL),$$

(3.17)

$$A_2 = C_{\lambda}R_f(d_{in} - d_{out} - S_s),$$

(3.18)

$$A_3 = 2R_qL(aR_qL - bC_{\lambda}R_f),$$

(3.19)

$$D_1 = \psi \left[ \frac{R_qL + C_{\lambda}d_{in}R_f}{C_{\lambda}R_fS_s} \right],$$

(3.20)

$$D_2 = \psi \left[ 1 + \frac{d_{out}}{S_s} + \frac{R_qL}{C_{\lambda}R_fS_s} \right],$$

(3.21)

and $\psi[\cdot]$ is the digamma function [202]. Note that (3.16) is valid for large diameter MWCNTs where both $d_{out}$ and $d_{in}$ are greater than $C_{Nc}$ where $C_{Nc}$ is the shell diameter below which the sub-bands in a semiconducting conducting shell do not appreciably contribute to the conduction ($C_{Nc} \approx 4 \text{ nm}$). For small diameter MWCNTs and SWCNTs ($d_{out} < C_{Nc}$ and $d_{in} < C_{Nc}$) where $N_c = 2P_m$ on average, (3.16) becomes

$$R_{ts} = \frac{-C_{\lambda}R_f^2S_s}{2P_m(A_2 + R_qL(D_2 - D_1))}.$$

(3.22)
When \( d_{out} > C_{Nc} \) and \( d_{in} < C_{Nc} \), the total resistance is the parallel combination of (3.16) and (3.22),

\[
R_{tm} = \frac{R_d[d_{out}, d_{in}][R_{ts}[d_{out}, d_{in}]]}{R_d[d_{out}, d_{in}] + R_{ts}[d_{out}, d_{in}]}
\]

(3.23)

where \( R_d[\cdot, \cdot] \) and \( R_{ts}[\cdot, \cdot] \) are (3.16) and (3.22) evaluated with the specified inner and outer diameters: \( d_{out} = d_{out}, d_{in} = d_{out} + S_s, d_{outs} = d_{in} + S_s[(C_{Nc} - d_{in})/S_s] \), and \( d_{ins} = d_{in} \). For general CNT bundles, the overall resistance \( (R_{tb}) \) is the resistance provided (3.16), (3.22), or (3.23) divided by \( N_b \). Note that the derivation of (3.16), (3.22), and (3.23) did not require the use of an integral approximation, and therefore, the equations provide an exact closed-form representation of (3.15). Note that the resistance of an SWCNT can be calculated using (3.22) assuming \( d_{in} = d_{out} = d_t \) where \( d_t \) is the diameter of the SWCNT.

### 3.2.6 Accuracy of the Resistance Model

To validate the proposed CNT resistance model, we compared the results from the model with experimental resistance measurements of SWCNTs [99,203], MWCNTs in an end contact configuration where all of the MWCNT shells are connected to the external electrodes [2,40], and MWCNTs in a side contact configuration where only the outermost MWCNT shell is connected to the external electrodes [144,148–150]. The results of the comparison are listed in Table 3.1. The CNT resistance model closely matches the experimentally reported resistance values for SWCNTs and MWCNTs in both the end and side contact configurations. Note that the small differences between
3.3 Capacitance Modeling

### 3.3.1 Quantum Capacitance

Carbon nanotubes have both quantum and electrostatic capacitances that can impact interconnect performance. The quantum capacitance ($C_q$) captures the energy necessary to add an extra conduction electron in a 1-D conductor modeled using previously reported experimental measurements, we can utilize the model to accurately and efficiently design high performance CNT-based interconnect solutions.

Given the favorable comparison between the closed-form CNT resistance model and physical parameters in the fabricated CNTs, which we discuss further in Chapter 6, the statistical variations in the number of metallic conducting MWCNT shells and other

<table>
<thead>
<tr>
<th>CNT Type</th>
<th>Contact Configuration</th>
<th>$L$ (nm)</th>
<th>$d_{CN}$ (nm)</th>
<th>$R_f$ (Ωf)</th>
<th>$C_q$ (aF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SWCNT</td>
<td>Side Contact</td>
<td>1.8</td>
<td>15</td>
<td>11.8</td>
<td>1.8</td>
</tr>
<tr>
<td>SWCNT</td>
<td>Side Contact</td>
<td>1.8</td>
<td>15</td>
<td>15.4</td>
<td>1.8</td>
</tr>
<tr>
<td>SWCNT</td>
<td>Side Contact</td>
<td>1.8</td>
<td>15</td>
<td>150</td>
<td>1.8</td>
</tr>
<tr>
<td>SWCNT</td>
<td>End Contact</td>
<td>1.8</td>
<td>15</td>
<td>28000</td>
<td>1.8</td>
</tr>
</tbody>
</table>

---

**Table 3.1:** Comparison of the CNT resistance model with published experimental results.

* - The experimentally reported contact resistance is multiplied by the number of conduction channels for an MWCNT shell of the given diameter to determine $R_f$.

---

* - Since no $X_{ap}$ values are reported in these papers, we assume the experimental $X_{ap}$ value reported in [149, 150] ($X_{ap} = 30$/JTO for a shell with a 15 nm diameter) and the MWCNT's outermost conducting shell.
Luttinger liquid theory [164]. The quantum capacitance has a theoretical value of \(4e^2/hv_F \approx 193 \text{ aF}/\mu\text{m}\) per conduction channel [166]. Therefore, the quantum capacitance for each shell of a CNT is

\[ C_q = \frac{4e^2}{hv_F} N_c L. \]  

(3.24)

The total quantum capacitance of all of the conducting shells in an CNT bundle is the parallel combination of the quantum capacitances of each MWCNT shell or individual SWCNT,

\[ C_{q\#} = N_b \sum_{j=1}^{N_s} C_{qj}, \]  

(3.25)

where \(C_{qj}\) is the quantum capacitance of the \(j\)th graphitic shell in a given CNT in the bundle calculated using (3.24). Since the quantum capacitance is significantly larger than the electrostatic capacitance for nanotube bundles and the quantum and electrostatic capacitances are in series in the CNT bundle circuit model displayed in Figure 3.2, the quantum capacitance typically has a small impact on the total capacitance of typical CNT bundle interconnect geometries [166].

### 3.3.2 Electrostatic Capacitance

The electrostatic capacitance of individual and bundled CNTs depends on the nanotube geometry and the geometry of the nearby metal and nanotube based conductors. Consequently, general purpose capacitance extractors such as FastCap [204]
or COMSOL [205] provide the most accurate means for characterizing the electrostatic capacitance of nanotube-based interconnect structures. However, for certain standard geometries, analytical formulations can be utilized to determine the electrostatic capacitance. In the following sections, we discuss capacitance modeling for several standard interconnect geometries for both individual and bundled CNT-based interconnect structures.

Individual Nanotubes

In the circuit model for individual CNTs displayed in Figure 3.1, the electrostatic coupling capacitance between adjacent concentric shells in an MWCNT is [206]

\[ C_c = \frac{2\pi \varepsilon L}{\ln \left( \frac{d_{out}}{d_{in}} \right)}. \]  

We only include the capacitive interaction between adjacent nearest neighbor concentric shells in an MWCNT since the electric fields are screened by the MWCNT shells [207]. Note that for typical interconnect applications, the effective contribution of \( C_c \) to the total capacitance will be negligible since the per unit length voltage drop across each conducting shell will be approximately equal. However, for nanotube-based capacitors, the inter-shell capacitance \( C_c \) may be significant depending on the contact configuration as we discuss in Chapter 8. The electrostatic coupling capaci-
The electrostatic capacitance between the outer shell of an isolated MWCNT or an individual SWCNT and a ground plane is

\[ C_g = \frac{2\pi \varepsilon L}{\ln \left( \frac{2(h_g - d_{out})}{2d_{out}} \right)} \quad (3.28) \]

where \( h_g \) is the distance between the outer shell of the MWCNT or individual SWCNT and the ground plane [164]. While (3.26)-(3.28) are useful for characterizing individual MWCNTs and SWCNTs, calculating the electrostatic capacitance of nanotube bundles requires more complex formulations.

**Nanotube Bundles**

For CNT bundles with a large number of small diameter MWCNTs or SWCNTs, the electrostatic coupling and ground capacitances of the bundle will be relatively close in value to the capacitance of a copper conductor with the same dimensions as the bundle with typical capacitance differences of 3% percent for bundles with densely packed nanotubes [29,175]. This is analogous and consistent with the capacitance results obtained for copper conductors with a certain level of surface roughness [175,208]. As the density of metallic nanotubes decreases, the electrostatic
capacitance can decrease by up to 15% from the capacitance value obtained from a copper conductor with the same dimensions as the nanotube bundle [175]. Therefore, existing capacitance models for copper conductors can be utilized as a basis for modeling the electrostatic capacitance of CNT bundles.

For rectangular interconnect in VLSI applications, parameterized models based on numerical electromagnetic simulations are typically utilized for the analytical evaluation of ground and coupling capacitance including the fringe capacitance between the conductors and the ground plane [209,210]. We utilize a modified version of the capacitance model for copper conductors presented in [210] to calculate the ground and coupling capacitances, $C_{gb}$ and $C_{cb}$ in Figure 3.1, for nanotube bundles consisting of SWCNTs or small diameter MWCNTs in this study. Note that we include the impact of the decreasing electrostatic capacitance from a decreased proportion of metallic nanotubes in the electrostatic capacitance model based on results from extensive electrostatic simulations using COMSOL Multiphysics for common CNT bundle interconnect geometries.

To enable rapid evaluation of electrostatic capacitance for CNT bundles consisting of one or two large diameter MWCNTs, we have developed a parameterized analytical model based on extensive field solver simulations using COMSOL Multiphysics. The model simultaneously captures the electrostatic capacitance between adjacent large diameter MWCNTs and to a ground plane for the interconnect geometries displayed in Figure 3.3. We employ the following geometric relations in the
Figure 3.3: Three interconnect configurations considered for the electrostatic capacitance model for large diameter MWCNT bundles.

analytical capacitance model:

\[
t_w = \frac{t_b}{w_b}, \quad t_s = \frac{t_b}{s_b}, \quad t_g = \frac{t_b}{h_g}, \quad s_w = \frac{s_b}{w_b}, \quad s_g = \frac{s_b}{h_g}, \quad h_w = \frac{h_g}{w_b}, \quad h_r = \frac{h_g + t_b}{t_b}, \quad s_{rat} = \frac{s_b + t_b}{t_b}
\]

(3.29)

where \(t_b\) and \(w_b\) are the height and width of the MWCNT interconnect structure, \(s_b\) is the edge-to-edge spacing between adjacent MWCNT interconnect structures, and \(h_g\) is the distance between the bottom of the MWCNT interconnect structure and the ground plane. The capacitance between the MWCNT interconnect structure and
the ground plane is

\[ C_{gb} = \frac{\varepsilon L}{1000} \left( \left( C_{cir1}^{\beta_3} + \frac{t_{w}^{\beta_6}}{C_{cir2}^{\beta_7}} \right) C_p^{\beta_8 + \beta_9 \varepsilon} \right) \]  

(3.30)

where

\[ C_{cir1} = \frac{\beta_1 \pi}{\ln(\beta_2 R)} \quad \text{and} \quad C_{cir2} = \frac{\beta_4 \pi}{\ln(\beta_5 R)} \]  

(3.31)

represent the logarithmic dependence of capacitance for circular conductors. For the \( C_{gb} \) case, \( R = h_{rat} \) in \( C_{cir1} \) and \( C_{cir2} \). The term

\[ C_p = \beta_{10} + \beta_{11} S_{w}^{\beta_{12}} + \beta_{13} t_{s}^{\beta_{14}} + \beta_{15} S_{g}^{\beta_{16}} + \beta_{17} t_{g}^{\beta_{18}} \]  

(3.32)

represents the capacitive behavior of interconnect structures that consist of one or two large diameter MWCNTs. \( C_p \) has a form typical of the parameterized models used for rectangular conductors [209,210]. The numerical values for \( \beta_{1} \cdots \beta_{18} \) used to calculate \( C_{gb} \) are determined using multivariate linear least squares regression and are listed in Table 3.2.

The capacitance \((C_{cb})\) between adjacent MWCNT interconnect structures is

\[ C_{cb} = C_{gb} C_{p2} + \frac{\varepsilon L}{1000} t_{w}^{\beta_{30}} C_{cir3}^{3} \]  

(3.33)
Table 3.2: Numerical values for the parameters in large diameter MWCNT bundle interconnect capacitance model.

where $C_{gb}$ is defined by (3.30), and

\[ C_{cir3} = \frac{\beta_{28} \pi}{\ln(\beta_{29} R)}. \]  \hspace{1cm} (3.34)

Note that $R = s_{rat}$ in $C_{cir1}$, $C_{cir2}$ and $C_{cir3}$ when calculating $C_{cb}$. $C_{p2}$ is defined as

\[ C_{p2} = \beta_{19} + \beta_{20} s_{w}^{\beta_{21}} + \beta_{22} s_{w}^{\beta_{23}} + \beta_{24} t_{s}^{\beta_{25}} + \beta_{26} t_{g}^{\beta_{27}}. \]  \hspace{1cm} (3.35)

The numerical values for $\beta_1 \cdots \beta_{30}$ used to calculate $C_{cb}$ are determined using multivariate linear least squares regression and are listed in Table 3.2. The capacitance model for $C_{gb}$ and $C_{cb}$ in (3.30) and (3.33) is valid for MWCNT-based interconnect geometries with one or two large diameter MWCNTs meeting the following conditions: $L \gg w_b, t_b; t_b = 0.5, 1, 2; 0.5 \leq s_b \leq 10$; and $0.5 \leq h_g \leq 50$. From an extensive set of field solver simulations using COMSOL Multiphysics, we find that
the average and maximum errors of the analytical model for $C_{gb}$ are 2.2% and 9.2%, respectively. The average and maximum errors for $C_{cb}$ are 1.9% and 9.1%, respectively. The proposed model provides an accurate and efficient means for evaluating the electrostatic capacitance of MWCNT-based interconnect structures.

3.4 Inductance Modeling

Carbon nanotubes have both kinetic and magnetic inductances that can affect interconnect delay, noise, and power consumption [29, 47, 49, 79, 156, 165]. In this section we discuss the modeling of inductance for individual and bundled CNTs.

3.4.1 Kinetic Inductance

In a 1-D conductor modeled based on Luttinger liquid theory [164], the kinetic inductance ($L_k$) captures the net sum of the kinetic energy of the left and right moving electrons in the nanotube, and as a result, it is a per unit length quantity. The kinetic inductance has a theoretical value of $\frac{\hbar}{4e^2v_F} \approx 8 \text{nH/\mu m}$ per conduction channel [165]. Therefore, the kinetic inductance for each shell of a CNT is

$$L_k = \frac{\hbar}{4e^2v_F} \frac{L}{N_c}. \quad (3.36)$$

Note that the theoretical value for kinetic inductance specified by (3.36) is on the same order as the values obtained in experimental measurements for the kinetic inductance.
of individual and bundled SWCNTs [160] and individual MWCNTs [156]. Since kinetic inductance is dependent on the kinetic energy in the nanotube, there is no kinetic inductance analog to partial mutual magnetic inductance. Consequently, the kinetic inductance can be modeled as an additional self-inductance [211–214].

The total kinetic inductance of all of the shells in an CNT bundle is the parallel combination of all of the $L_k$ values for the individual MWCNT shells or SWCNTs,

$$L_{kb} = \frac{1}{N_b \sum_{j=1}^{N_s} \left( \frac{1}{L_{kj}} \right)} ,$$  \hspace{1cm} (3.37)

where $L_{kj}$ is the kinetic inductance of the $j$th shell in a given CNT in the bundle calculated using (3.36). Therefore, like resistance, kinetic inductance is substantially reduced as $N_b$ is increased, which was experimentally verified in [160]. Note that the kinetic inductance will typically not have a major impact on SWCNT-based interconnect performance for operating frequencies below 50 GHz as discussed in Section 5.1 and experimentally examined for SWCNTs in [140, 160].

### 3.4.2 Magnetic Inductance

The magnetic inductance captures the impact of the voltage induced by the magnetic fields produced by time varying currents, which is encapsulated in Ampere’s and Faraday’s laws [79]. Unlike resistance, capacitance, and kinetic inductance, magnetic inductance is dependent on the entire current loop, which typically consists of a signal
Figure 3.4: System of carbon nanotube interconnect bundles implementing a signal line and two adjacent ground return paths (ground-signal-ground (GSG) configuration).

line and its associated ground return paths as depicted in Figure 3.4 [215]. Since the distribution of the current in the loop may not be known a priori, the concept of partial inductance is used to model the magnetic inductance. Partial inductance is a mathematical construct that assumes that the current flowing a particular conductor, in the case of partial self inductance, or the current flowing in adjacent conductors, in the case of partial mutual inductance, has a current return path at infinity. The partial inductance construct has no physical meaning by itself. However, when the partial self and mutual inductances are combined in a particular manner over an entire current loop, the total loop inductance, which is the physical inductance that impacts delay, noise, and power consumption, can be calculated [215].

Assuming that each individual MWCNT shell or metallic SWCNT is current carrying filament, the partial self inductance \( L_m \) of an individual MWCNT shell or
metallic SWCNT is the summation of its internal \( L_{int} \) and external \( L_{ext} \) inductances. The external inductance of a current carrying circular ring is

\[
L_{ext} = \frac{\mu L}{2\pi} \left( \ln \left( \frac{2L}{r} \right) - 1 \right)
\]  

(3.38)

where \( r \) is the radius of the ring [182]. Assuming that the thickness of the circular ring is much less than its radius, which is the case for an individual MWCNT shell or SWCNT, \( L_{int} \approx 0 \). Therefore, the self inductance \( (L_m) \) of each individual MWCNT shell or SWCNT is equal to \( L_{ext} \) in (3.38).

The partial mutual inductance between individual MWCNT conducting shells or between individual SWCNTs can be determined based on the partial mutual inductance between two carrying filaments. The partial mutual inductance \( (M_m) \) between two concentric conducting shells in an individual MWCNT is

\[
M_m = \frac{\mu L}{2\pi} \left( \ln \left( r + \sqrt{1+r^2} \right) - \sqrt{1 + \left( \frac{1}{r} \right)^2} + \frac{1}{r} \right)
\]  

(3.39)

where \( r = L/\max(r_1, r_2) \), and \( r_1 \) and \( r_2 \) are the radii of the shells [216]. The effective distance between the two current carrying filaments is \( \max(r_1, r_2) \) since the flux linkage between the two concentric rings is zero inside the ring with the largest radius. The quantity \( r = L/D_{GMD} \) can be substituted for \( r \) in (3.39) to determine the mutual inductance between individual MWCNT conducting shells or between individual SWCNTs in adjacent CNTs \( (M_{mm}) \). Using a contour integration method, \( D_{GMD} \),
which is the geometric mean distance between graphitic shells, has been proven to be
equivalent to the center-to-center distance between individual MWCNT conducting
shells or between individual SWCNTs [217]. When compared with results from the
field solver, FastHenry [218], the inductance model has a maximum error of 0.6% over
a wide-range of simulated CNT geometries.

Once the self and mutual inductance values for each individual MWCNT shell
or SWCNT in the CNT interconnect system are calculated, they can be combined
into a partial inductance matrix to determine the total loop inductance \( L_{\text{loop}} \), which
encapsulates \( L_{mb} \) and \( M_{mb} \) in the aggregated circuit model for the CNT bundle inter-
connect wires displayed in Figure 3.2, if all of the significant ground return paths are
modeled. To determine the loop inductance for CNT bundle-based interconnect, we
utilize the Partial Element Equivalent Circuit (PEEC) method [215,218]. In order to
apply the PEEC method to CNT bundles, we model the individual MWCNT shells or
SWCNTs in the bundle as individual current carrying filaments. We call this modeling
method the \textit{equivalent conductor model}. Using a conservation of energy approach,
the loop inductance for the signal bundle and its parallel ground return bundles is

\[
L_{\text{loop}} = i_t^T L_{\text{mat}} i_t = i_t^T \begin{bmatrix}
  L_{m1} & M_{m12} & \cdots & M_{m1n} \\
  M_{m21} & L_{m2} & \cdots & M_{m2n} \\
  \vdots & \vdots & \ddots & \vdots \\
  M_{mn1} & M_{mn2} & \cdots & L_{mn}
\end{bmatrix} i_t
\]
where \( \mathbf{i}_t \) is a vector with the normalized current in each individual MWCNT shell or SWCNT, \( L_{\text{mat}} \) is the partial inductance matrix, \( L_{\text{mi}} \) are the partial self-inductance values for the interconnect system (\( L_m \) in Figure 3.1) calculated using (3.38), and \( M_{\text{mij}} \) are the partial mutual inductance values between individual MWCNT conducting shells or between individual SWCNTs (\( M_m \) and \( M_{mm} \) in Figure 3.1) calculated using (3.39). For low complexity systems of SWCNT bundles, (3.40) can be used directly to calculate the loop magnetic inductance. However, since we want to analyze the accuracy of the inductance models for a wide-range geometries, we utilize the multipole-accelerated field solver, FastHenry, which uses a PEEC formulation similar to \( L_{\text{loop}} \) [218]. For applications where the high frequency current distribution in the interconnect bundles plays an important role, such as for on-chip inductors, we extend the PEEC formulation in (3.40) to include the resistance of each individual MWCNT shell or SWCNT as we discuss in Chapter 7.

Given the large number of individual MWCNT shells or SWCNTs in a given CNT bundle-based interconnect structure, the size of the matrix \( L_{\text{mat}} \) in (3.40) can become large, which limits the size of the interconnect structure that can be modeled in a computationally feasible manner. To more efficiently model the magnetic inductance, we have developed the equivalent conductivity model, which approximates the magnetic inductance of the discrete CNTs in the bundle with one conductor that has the same dimensions and conductance as the nanotube bundle. The conductor can have multiple current-carrying filaments to more accurately model the inductance.
Table 3.3: Results for magnetic inductance models.

To evaluate the speed and accuracy of the equivalent conductivity model for magnetic inductance, we performed 2500 simulations on the GSG conductor configuration for a wide-range of realistic SWCNT bundle geometries for future process technologies as predicted by ITRS [1]. The geometric parameters have the following ranges of values: $10 \mu m \leq L \leq 5000 \mu m$, $10d_t \leq w_b \leq 20d_t$, $d_t \leq b \leq 20d_t$, $0.1w_b \leq s_b \leq 1000w_b$, and $1 GHz \leq f \leq 20 GHz$ where $f$ is the operating frequency for the interconnect, and $s_b$ is the edge-to-edge spacing between the signal and ground bundles. Note that for this set of experiments, the bundle consists of SWCNTs with $d_t = 1 nm$ and the SWCNTs are assumed to be densely packed. Table 3.3 lists the maximum and mean errors of the equivalent conductivity model with respect to the discrete equivalent conductor model. The equivalent conductivity model with 5 filaments achieved a maximum error of 6.49% with typical errors of 0.80%. These errors are within the manufacturing tolerances of future SWCNT bundle interconnect technology. Note that we similar results for the magnetic inductance of MWCNT bundle based interconnect modeled using the equivalent conductivity model. We also compare the magnetic inductance models to previous expressions that only model the self inductance for the SWCNTs in the bundle [168]. These previous models signif-
Figure 3.5: CPU time as the number of nanotubes per dimension in the SWCNT bundle increases. The equivalent conductivity model provides a scalable magnetic inductance modeling solution.

In terms of CPU time, once the number of SWCNTs per dimension in a bundle exceeds 30 for the GSG configuration, calculating the loop magnetic inductance using the equivalent conductor model becomes intractable as depicted in Figure 3.5. For evaluating CNT bundles with a large number of nanotubes, which is necessary to reduce the overall resistance of the bundle, the equivalent conductivity model must be utilized. Therefore, the equivalent conductivity model provides a scalable solution for the magnetic inductance modeling of CNT bundles.
Chapter 4

Investigating the Resistance of CNT-Based Interconnect

Since the lower resistance of CNTs is one of the major electrical advantages associated with CNT-based interconnect, we comprehensively investigate and compare the resistance of CNT and copper-based interconnect solutions in this chapter. We examine the impact of nanotube specific properties on the resistance of SWCNT-based interconnect solutions in Section 4.1. We also compare the resistance of SWCNT bundles and copper interconnect in this section. In Section 4.2, we compare the resistance of MWCNT-based interconnect of different diameters with scaled copper interconnect. Finally, in Section 4.3, we investigate the modeling and resistance impact of partially connected and fully disconnected SWCNTs and MWCNT shells in nanotube-based interconnect solutions. The results from this investigation will be
leveraged when determining the optimal design of CNT-based solutions for on-chip communication and for passive components in Chapters 5, 7, and 8.

4.1 SWCNT Bundle Resistance

4.1.1 Diameter-Dependent Ohmic and Contact Resistances

The diameter dependence of the ohmic and contact resistance of an individual SWCNT has interesting implications for the design of SWCNT bundle interconnect and its suitability as a replacement for traditional copper interconnect as process technology scales. To investigate the diameter-dependent impact of effective ohmic resistivity of the SWCNT bundle, we calculate the resistance per unit length and...
Figure 4.2: Effective ohmic resistivity versus $d_t$ for dense ($P_m = 1$) and sparse ($P_m = 1/3$) SWCNT bundles modeled with and without the diameter-dependent resistance formulation. The resistivity of bulk copper and predicted resistivity of global copper wires with minimum pitch in the 45 nm and 22 nm process technologies are shown for reference [1].

$\lambda_{ap}$ for SWCNTs of various diameters, which are depicted in Figure 4.1. As $d_t$ is increased, $\lambda_{ap}$ increases linearly, which corresponds to a $1/\lambda_{ap}$ decrease in resistance [44]. The resistance per unit length for carbon nanotubes is proportional to $1/d$ while for standard copper conductors the resistance has a $1/d^2$ dependence at low frequencies. Therefore, the resistance of SWCNTs is proportional to the surface area of the nanotube. In contrast, the resistance of a metallic conductor is proportional to the cross-sectional area of the conductor.

We also calculate the per unit area ohmic resistivities of both densely ($P_m = 1$) and sparsely ($P_m = 1/3$) packed SWCNT bundles, which are depicted in Figure 4.2 for $d_t$ values ranging from 0.4 nm to 4.0 nm [41, 98, 219]. Note that $d_t$ values
of 0.8 to 1.0 nm at least are needed to provide both mechanical stability and good electrical conductivity [220]. For comparison purposes, we plot the resistivity of bulk copper and predicted resistivity of global copper wires with minimum pitch in 45 nm and 22 nm process technologies [1]. To highlight the comparison between the ohmic resistance of copper and SWCNT bundles, we neglect the contact resistance for this experiment, which is valid for relatively long interconnect lengths.

The densely packed SWCNT bundles with diameters less than 2.2 nm have an effective resistivity that is less than that of bulk copper. For nanotube diameters up to 4.0 nm in the densely packed case, the effective resistivity of the bundle is less than the predicted resistivity of minimum pitch copper wires in both 45 nm and 22 nm process technologies. For sparsely packed nanotube bundles, the effective resistivity reaches that of bulk copper when the nanotube diameter reaches 0.75 nm. The effective resistivity reaches the predicted resistivity of minimum pitch copper wires in 45 nm and 22 nm technologies when the nanotube diameter is 1.4 nm and 2.0 nm, respectively. Consequently, SWCNT-based interconnect solutions can provide significantly lower resistance than copper interconnect, particularly as the cross-sectional dimensions of the copper conductors scale downward in future process technologies.

To evaluate the importance of modeling the dependence of $d_t$ on SWCNT resistance, we also plot the effective ohmic resistance for bundles with a nanotube diameter-independent resistance, which was assumed in previous SWCNT bundle models [164–172], in Figure 4.2. The percentage difference in ohmic resistance be-
Figure 4.3: Percentage difference between the diameter-dependent and fixed diameter-independent resistances for both ohmic and contact resistance.

The difference between the diameter-dependent formulation and diameter-independent models is displayed in Figure 4.3. The results indicate that neglecting the diameter-dependent nature of the ohmic resistance can produce errors as high as 120 percent. For bundles of nanotubes with small diameters, assuming a diameter independent resistance significantly underestimates the effective ohmic resistivity of the nanotube. In contrast, for bundles of nanotubes with large diameters, the resistivity is overestimated.

To determine the effect of the diameter-dependent contact resistance on SWCNT bundles, we calculate the contact resistance of bundles with different individual nanotube diameters and bundle width values. The calculated contact resistances, normalized to the contact resistance of a single SWCNT with large diameter \( R_{cnm} \), are depicted in Figure 4.4 for densely packed nanotube bundles \( P_m = 1 \). For sparse bundles, the normalized contact resistance values are three times larger if \( P_m = 1/3 \). The
Figure 4.4: Contact resistance of an SWCNT bundle with the specified nanotube diameters normalized to the contact resistance of an individual SWCNT.

The percentage difference in contact resistance between the proposed diameter-dependent formulation and previous diameter-independent models is displayed in Figure 4.3. The diameter-dependent contact resistance produces significantly higher overall contact resistances for the bundles with nanotubes diameters less than 1.8 nm. For $d_t = 1 \text{ nm}$, neglecting the diameter dependence on contact resistance underestimates the resistance by 85 percent. Therefore, to accurately determine the relative performance of CNT bundles and traditional copper interconnect, the diameter-dependent resistance of the CNTs must be taken into account.

### 4.1.2 Total SWCNT Bundle Resistance

To examine the impact of the overall SWCNT bundle resistance for realistic interconnect geometries, we calculated the total resistance of dense SWCNT bundles for
Figure 4.5: Percentage improvement in SWCNT bundle resistance over copper interconnect resistance for typical interconnect geometries.

various bundle length and width values, $d_t = 1.0 \text{ nm}$, $R_{\text{enom}} = 20 \text{ k}\Omega$, and $I_o = 20 \mu\text{A}$. We assume that the supply voltage is 0.8 V and the driver resistance is 2.5 kΩ, which are predicted by ITRS for the 22 nm process technology [1]. The maximum voltage drop across an SWCNT bundle for a particular supply voltage and driver resistance was formulated based on [171]. The results are displayed in Figure 4.5. The percentage improvement in resistance obtained by using SWCNT bundles can be categorized based on the width and length of the bundles. For long bundles with large widths, the contact resistance of the bundle is insignificant, and the nanotube bundle completely benefits from the decrease in effective resistivity displayed in Figure 4.2. For $d_t = 1.0 \text{ nm}$, the overall resistance is decreased by 61 percent over copper interconnect. For long bundles with small widths of approximately 22 nm, this improvement in resistance increases to 82 percent due to the increase in copper resistivity.
SWCNT bundles are at a disadvantage for short interconnect lengths and large widths, when the contact resistance is significant compared to the ohmic resistance and the resistivity of the standard copper interconnect is near its bulk value. For short bundle lengths with narrow widths, the increased resistivity of standard copper interconnect can cause the SWCNT interconnect to become more favorable despite its large contact resistance. However, the bundles with short lengths and wide widths no longer produce better performance since the relatively wide copper interconnect has resistivity close to that of bulk copper.

$P_m$ and $d_t$ also have an important impact on CNT bundle resistance. For the narrow bundle width of 22 nm depicted in Figure 4.6a, SWCNT bundles have the same resistance as their equivalent copper counterparts for bundles with individual
Figure 4.7: Bundle length and nanotube diameter where the percentage improvement in SWCNT bundle resistance over copper interconnect resistance is zero for $w_b = 22, 50,$ and $200$ nm. Note that the bundle has a optimum $d_t$ value.

nanotubes diameters ranging from $2.2$ nm to $1.4$ nm for $P_m$ values ranging from $1$ to $1/3$. For wider bundles with $w_b = 200$ nm, depicted in Figure 4.6b, SWCNT bundles and copper interconnect have the same resistance for individual nanotubes diameters ranging from $1.7$ nm to $0.95$ nm for $P_m$ values ranging from $1$ to $1/3$.

Figure 4.7 depicts the bundle length and nanotube diameter where the percentage improvement in SWCNT bundle resistance over copper interconnect resistance is zero for various bundle width configurations. Two conflicting design parameters impact the minimum interconnect length where SWCNT bundles have an advantage in resistance over copper interconnect. As the nanotube diameter is decreased, the contact resistance of the individual SWCNTs substantially increases as described in Section 3.2.1. However, the number of nanotubes in the bundle increases as the nanotube diameter decreases, which leads to lower overall resistance. Due to the interaction
between these two conflicting trends, an optimum individual nanotube diameter exists, and the optimal \( d_t \) is greater than the minimum feasible \( d_t \) values for bundles with relatively small \( L \) values.

### 4.2 MWCNT Bundle Resistance

Given the importance of the SWCNT diameter and length in determining the overall resistance of nanotube bundles, which we discuss in the previous section, we examine the resistance of MWCNTs versus nanotube diameter and length in this section. The resistivity of a nanotube bundle is

\[
\rho_M = \frac{\sqrt{3}}{2} \frac{R_{tot}}{L} (d_{out} + S_t)^2
\]  

(4.1)

where \( R_{tot} \) is given by either (3.16), (3.22), or (3.23) depending on \( d_{out} \) and \( d_{in} \). Note that the factor of \( \sqrt{3}/2 \) accounts for the hexagonal lattice geometry of the nanotubes in the bundle [108].

To assess the impact of nanotube diameter on resistance, we simulated the resistivity of an MWCNT bundle for various \( L \) values. Figure 4.8 displays the resistivity of an MWCNT bundle versus \( d_{out} \) for various MWCNT bundle lengths. We assume that \( R_f = 20 \, k\Omega \), \( S_t = 0.34 \, nm \), and \( d_{in}/d_{out} = 0.5 \). MWCNTs can provide lower resistivity than copper interconnect depending on the value of \( L \) and \( d_{out} \). For a fixed length with \( L \leq 10 \, \mu m \), the smallest possible \( d_{out} \) values provide the lowest resistivity,
while for $L \geq 20 \, \mu m$, the largest possible $d_{out}$ values provide the lowest resistivity. We observe this general trend for a large range of $R_f$, $S_t$, and $d_{in}/d_{out}$ values.

Physically, the nanotube length value plays an important role in determining the resistance of MWCNTs due to $R_f$. In general, for short $L$ values, the resistivity of large diameter MWCNTs is greater than the resistivity of small diameter MWCNTs since the large diameter shells of the MWCNTs have relatively large $\lambda_{op}$ values that result in ballistic conduction where $R_{ib}$ and $R_{cb}$ dominate $R_{ob}$. For larger $L$ values, large diameter MWCNTs can have lower resistivity than small diameter MWCNTs since $\lambda_{ap}$ is greater for conducting shells with larger diameters. Therefore, the optimal outer diameter in terms of resistance for short length MWCNTs is the smallest feasible diameter, and the optimal outer diameter for long length MWCNTs is the largest feasible diameter. We exploit this property when developing optimal design solutions for CNT-based interconnect in Section 5.2.
4.3 Resistance of Partially Contacted Nanotubes

In nanotube-based interconnect solutions, some of the individual SWCNTs in an SWCNT bundle or some of the individual shells in an MWCNT may not be well-connected to the external metal electrodes [103, 221]. As depicted in Figure 4.9 for an SWCNT bundle, some of the individual SWCNTs may be fully connected to the metal electrodes on both ends of the bundle, partially connected to only one of the metal electrodes at the end of the bundle, or fully disconnected from both of the metal electrodes attached to the bundle. The shells of an MWCNT can be classified in the same manner with respect to their connections with the metal electrodes at the ends of the MWCNT. In the following sections, we discuss the modeling and resistance impact of partially connected and fully disconnected SWCNTs and MWCNT shells.
4.3.1 Modeling of Partially Contacted Nanotubes

To understand the impact of partially contacted nanotubes on the resistance of CNT-based interconnect structures, we model SWCNT bundles and MWCNT shells utilizing the distributed resistance model displayed in Figure 4.9, which is based on the resistances considered in the full RLC circuit model for nanotube-based interconnect presented in Figure 3.1. The ohmic and high bias resistances are modeled in a distributed manner with

\[ R_D = \frac{R_o + R_{hb}}{n_d} \]  \hfill (4.2)

where \( n_d \) is the number of distributed segments used to model the per unit length resistance of the nanotubes. Utilizing a sufficiently large \( n_d \) value when constructing the distributed resistance model is critical since current can potentially flow between nanotubes when partially or fully disconnected SWCNTs are present. In practice, we find that setting \( n_d = 20 \) provides a good trade-off between accuracy and computational complexity. Similar to (4.2), the distributed inter-tube resistance used in the model is calculated based on

\[ R_{tD} = \frac{R_t}{n_d + 1}. \]  \hfill (4.3)

When the nanotubes are connected to the external metal contacts, the total contact resistance is

\[ R_C = \frac{R_c + R_t}{2}. \]  \hfill (4.4)
The nanotubes that are not connected to the metal contacts still have an intrinsic resistance where \( R_I = R_t/2 \). Note that the distributed and lumped resistance associated with the shells in an MWCNT are calculated in a similar manner to (4.2)-(4.4). Figure 4.9 depicts the resistance model for a bundle with fully connected, partially connected, and fully disconnected nanotubes.

Once the resistor values in the distributed resistance model are determined, we solve for the overall resistance of the bundle using a nodal analysis formulation where we calculate the voltage across each resistor in the circuit and the input port currents for a given applied bias voltage to the ports. Note that the two input ports of the distributed resistance model, which are indicated by the open circles in the model depicted in Figure 4.9, correspond to the two external metal contacts of the nanotube-based interconnect structure. For a resistor network consisting of \( n_n \) nodes, we solve the following matrix equation for the node voltages contained in the vector \( \mathbf{v} \) (\( n_n \times 1 \) vector) and for the port currents contained in the 2 x 1 vector \( \mathbf{i}_p \):

\[
\begin{bmatrix}
AGA^T & A_p \\
A_p^T & 0
\end{bmatrix}
\begin{bmatrix}
\mathbf{v} \\
\mathbf{i}_p
\end{bmatrix}
= 
\begin{bmatrix}
0 \\
\mathbf{v}_p
\end{bmatrix}
\]  

(4.5)

where \( A \) is the incidence matrix \( (n_n \times n_r) \) associated with the \( n_r \) resistors in the circuit, \( G \) is a diagonal matrix \( (n_r \times n_r) \) with the inverse value of each resistor \((1/R)\) on the diagonal, \( A_p \) is the incidence matrix \( (n_n \times 2) \) for the voltage sources that are assumed to exist at the two ports, and \( \mathbf{v}_p \) is a vector \((2 \times 1)\) containing the
4.3.2 Resistance of Partially Contacted SWCNTs

In order to understand the resistance implications of partially contacted nanotubes, we simulated the resistance of two adjacent SWCNTs with \( d_t = 1.4 \) nm, \( R_i + R_c = 10 \) k\( \Omega \), and various \( L \) and \( S_t \) values. Figure 4.10a depicts the total ohmic resistance of one of the SWCNTs and the overall coupling resistance between the two SWCNTs for various \( S_t \) values. The SWCNT ohmic and coupling resistances are comparable when \( L \) is approximately 9 \( \mu m \), 25 \( \mu m \), and 120 \( \mu m \) for \( S_t \) values of...
0.34 nm, 1 nm, and 2 nm, respectively. The increase in $S_t$ exponentially enlarges the coupling resistance between the two SWCNTs since the tunneling distance between the adjacent nanotubes is increased based on (3.13).

The relative values of the ohmic and coupling resistances play an important role in determining the contribution of partially connected and disconnected SWCNTs to resistance. Figure 4.10b depicted the overall resistance of the two adjacent SWCNTs with various contact configurations and nanotube spacing values normalized to the resistance of an individual SWCNT. For small $L$ values, the coupling resistance between the SWCNTs is significantly larger than the ohmic resistance of the fully connected SWCNT. Therefore, the current primarily remains in the fully connected SWCNT and the partially connected / disconnected SWCNTs do not significantly contribute to the conduction in the 2 parallel SWCNT system. As a result, the normalized overall resistance remains approximately 1. For $L$ values where the ohmic and coupling resistances are comparable, the partially connected / disconnected SWCNTs begin to contribute to conduction and the normalized resistance of the 2 nanotube system begins to decrease. For large $L$ values where the ohmic resistance is significantly larger than the coupling resistance, the normalized resistance approaches 0.5, which signifies that both the fully connected SWCNT and the partially connected / disconnected SWCNT in the 2 nanotube system are equally contributing to reduce the resistance.

The length of the partially connected / disconnected SWCNTs relative to $L$ also plays an important role in the resistance of the 2 nanotube system. Figure 4.11a
Figure 4.11: (a) Resistance of 2 SWCNTs with various contact configurations and various length values for the disconnected SWCNT normalized to the resistance of an individual SWCNT. (b) Resistance of an SWCNT bundle with various percentages of the SWCNTs connected to the external contacts normalized to the resistance of an SWCNT bundle with all of the individual SWCNTs connected to the external contacts.

depicts the resistance of the 2 nanotube system normalized to the resistance of an individual SWCNT. In this set of simulations, the disconnected SWCNT has several different length values that are reported in relative terms to $L$, and $S_t = 0.34$ nm. When the disconnected SWCNT has a shorter length value, this increases the coupling resistance, which increases the length at which the disconnected SWCNT will begin to significantly contribute to the overall conduction. For large $L$ values, the resistance reduction due to the disconnected SWCNT is inversely proportional to its length.

The general trends associated with the 2 nanotube system also apply to larger SWCNT bundles. We utilized the distributed resistance model to determine the overall resistance of an SWCNT bundle with $R_t + R_c = 10$ kΩ, $P_m = 1/3$, $w_b = 22$ nm, $t_b = 44$ nm, $S_t = 0.34$ nm, and $d_t = 1.4$ nm. Figure 4.11b displays the resistance of an SWCNT bundle with various percentages of the SWCNTs connected to the external contacts normalized to the resistance of an SWCNT bundle with all of
the individual SWCNTs connected to the external contacts. For small $L$ values, the disconnected SWCNTs do not contribute to the conduction and the resistance of the bundle is equivalent to the parallel resistance of the fully contacted SWCNTs only. As $L$ is increased, the disconnected SWCNTs begin to contribute to the conduction and lower the resistance, which eventually becomes equal to the resistance of the SWCNT bundle with all of the metallic SWCNTs connected to the external contacts.

### 4.3.3 Resistance of Partially Contacted MWCNTs

MWCNTs with disconnected shells exhibit similar behavior to SWCNT bundles with disconnected SWCNTs. We simulated the resistance of an MWCNT with 2 metallic shells and various outer diameters. The outer shell is connected to both external contacts while the inner shell is disconnected from both contacts. The resistance of the 2 shell MWCNTs normalized to the resistance of 1 shell MWCNTs with the corresponding diameters is displayed in Figure 4.12a. The overall resistance of the 2 shell MWCNTs with disconnected inner shells have a similar trend to the resistance of the aforementioned 2 SWCNT system. The MWCNTs with small $L$ values have resistance values that are close to the resistance values of 1 shell MWCNTs while the MWCNTs with large $L$ values have resistance values that approach the resistance values of two shell MWCNTs with both shells connected to the external contacts.

To extend the results from the 2 shell MWCNT case to a more realistic interconnect structure, we simulated the resistance of an MWCNT with an outer diameter of
Figure 4.12: (a) Resistance of 2 shell MWCNTs with the outer shell connected to the external contacts for various outer diameters normalized to the resistance of 1 shell MWCNTs with the corresponding diameters. (b) Resistance of an MWCNT with a 22 nm diameter (17 shells) and various contact configurations for the individual shells normalized to the resistance of a single MWCNT shell with a 22 nm diameter.

22 nm and an inner diameter of 11 nm, which results in an MWCNT with 17 shells. In this case we assume that $P_m = 1/3$ and utilize Monte Carlo simulation to randomly place the connected and disconnected metallic and semiconducting MWCNT shells.

Figure 4.12b displays the average resistance of an MWCNT with a 22 nm diameter and various contact configurations for the individual shells normalized to the average resistance of a single MWCNT shell with a 22 nm diameter. The resistance of the 17 shell MWCNT show the same trend as the resistance of the 2 shell MWCNT and the SWCNT bundles with respect to $L$. Therefore, in general in both the SWCNT and MWCNT cases, the disconnected SWCNTs / MWCNT shells do not contribute to current conduction for small $L$ values while for large $L$ values, the disconnected SWCNTs / MWCNT shells contribute to the current conduction to the same degree as a fully connected SWCNT / MWCNT shells due to the interplay between the ohmic and coupling resistances.
In this chapter, we investigate the design and performance of carbon nanotube interconnect for on-chip communication in digital VLSI applications. Leveraging the generalized RLC circuit model for CNT bundle-based interconnect discussed in Chapter 3 and the insights into the resistive behavior of CNT bundles discussed in Chapter 4, we first investigate the performance of nanotube-based interconnect versus important geometric and process parameters, mainly focusing on SWCNT bundle-based solutions, in Section 5.1. We then develop a optimal design methodology for generalized MWCNT/SWCNT-based interconnect solutions in Section 5.2. Finally, in Section 5.3, we discuss the performance of optimized MWCNT/SWCNT bundle-based interconnect solutions and examine what fabrication requirements must be
met for CNT interconnect to be a competitive solution compared to scaled copper interconnect in future process technologies.

5.1 Performance of SWCNT Bundle Interconnect

In this section, we examine the performance of SWCNT bundles for VLSI applications. We extract the RLC model for the GSG interconnect configuration depicted in Figure 3.4 using the modeling techniques described in Chapter 3. We then perform HSPICE simulations on the extracted RLC netlist with driver parameters and load capacitances specified by [1] to determine the delay and current density for the simulated SWCNT bundle configurations. We examine the performance of local interconnect with relatively short wire length values used to connect standard cells in VLSI systems and the performance of global interconnect with relatively long wire length values used to connect large circuit blocks across a given VLSI design. Note that the general performance trends presented in this section for SWCNT bundle interconnect are closely related to the general performance trends for MWCNT bundle-based interconnect. We examine the performance of MWCNT bundle-based interconnect in greater detail in Section 5.3.

5.1.1 Local Interconnect Delay and Current Density

To evaluate the performance of SWCNT bundles for local interconnect, we simulated different configurations with varying $d_t$, $R_{cnoa}$, $L$, and $P_m$ values. We use the
Figure 5.1: Maximum current density per nanotube (μA) versus (a) $d_t$ and $R_{cnom}$ and (b) $P_m$ and $L$ for local interconnect.

The current density is the largest when the total contact resistance ($R_i + R_c$) is near its intrinsic value ($R_i$) and $d_t$ is large. When $d_t = 2 \text{ nm}$ and $R_i + R_c = 6.5 \text{ k}\Omega$, the maximum current density is $3.5 \mu\text{A}$ per nanotube, which is significantly lower than the 20 $\mu\text{A}$ maximum current density for nanotubes with 2 $\text{nm}$ diameters and also lower than the 5 $\mu\text{A}$ maximum current density for nanotubes with 1 $\text{nm}$ diameters. Figure 5.1b depicts the maximum current density per nanotube versus $P_m$ and $L$ for local interconnect with $d_t = 1.5 \text{ nm, } R_{cnom} = 20\text{k}\Omega$, and $f = 10 \text{ GHz}$. The maximum...
current density per nanotube was 2.9 $\mu$A for the range of values simulated, which is also well below the limit for SWCNTs. Therefore, the nominal current density in SWCNT bundles in local interconnect does not pose a significant performance or reliability issue. We obtain similar results for the current density in global interconnect.

In terms of delay, the SWCNT bundle performance relative to standard copper interconnect primarily depends on $R_{\text{cnom}}$, $L$, and $P_m$. Figure 5.2 depicts the percentage improvement in SWCNT bundle delay over standard copper interconnect versus $P_m$ and $L$ for local interconnect with $d_t = 1.5$ nm and $R_{\text{cnom}} = 20$ k$\Omega$. For short interconnect length values, the standard copper interconnect has less delay than SWCNT bundle interconnect since the fixed contact resistance of the SWCNTs dominates the overall resistance. However, the negative resistive impact of the short SWCNT bundles is offset by the effective resistance of the interconnect driver circuit.
For longer interconnect, the advantage of the improved ohmic resistance of SWCNT bundle interconnect over standard copper interconnect leads to an improvement in delay, especially in bundles where a large percentage of the nanotubes are metallic. Furthermore, the longer bundle length increases the overall interconnect resistance, which reduces the relative impact of driver and contact resistances.

### 5.1.2 Global Interconnect Delay and Current Density

To evaluate the performance of SWCNT bundles for global interconnect, we simulated interconnect configurations with varying $d_t$ and $P_m$ values. Figure 5.3 displays the percentage improvement in SWCNT bundle delay over standard copper interconnect versus $P_m$ and $d_t$ for global interconnect with $L = 1 \text{ mm}$. Both $P_m$ and $d_t$ have a large impact on SWCNT bundle delay, which primarily stems from the relative
Figure 5.4: Percentage improvement in SWCNT bundle delay over standard copper interconnect versus bundle width and the width-to-bundle separation ratio when inductive effects are taken into account.

difference in resistance between SWCNT and copper technology depicted in Figure 4.2. For small individual nanotube diameters, the SWCNT bundle has less delay than standard copper interconnect for the full range of $P_m$ values (1/3 to 1). However, for larger individual nanotube diameters, $P_m$ will determine if SWCNT bundles offer a performance advantage over standard copper interconnect. Therefore, based on the delay results presented in Figure 5.3, developing techniques that control the diameter and chirality of SWCNTs will be vital for the effective utilization of SWCNT bundles for global interconnect applications [31,109,113,223,224].

5.1.3 Impact of Inductance on Delay in SWCNT Bundles

Given the importance of inductive effects for global interconnect in standard copper technology for both performance and reliability [6,81], we investigate the impact
of inductance on SWCNT bundle interconnect. Figure 5.4 displays the percentage improvement in SWCNT bundle delay over standard copper interconnect versus $w_b$ and the width-to-bundle separation ratio when inductive effects are taken into account. We assume that $P_m = 1$, $d_t = 1 \text{ nm}$, and $L = 1 \mu m$. For bundle width values of less than 100 nm and a width-to-bundle separation ratio between the signal and ground lines of less than 10, the performance improvement of the SWCNT bundles closely matches the improvement in resistance displayed in Figure 4.5. For interconnect with these geometries, the resistance dominates the overall impedance ($R \gg \omega L$). Therefore, the decreased resistance of the SWCNT bundles largely determines the delay enhancement. For larger SWCNT bundle width values, which result in decreased resistance, or larger width-to-separation ratios, which results in increased inductance, the relative improvement in the delay of the SWCNT bundle over standard copper
interconnect decreases since the inductance begins to dominate the overall resistance ($R \ll \omega L$). Since the inductance of the SWCNT bundle is typically greater than or equal to that of standard copper interconnect, the SWCNT bundle interconnect loses its delay advantage over standard copper interconnect for large bundle width values.

Inductive effects can also cause voltage overshoot, which can damage transistors and cause logic failures [6, 81]. Figure 5.5 displays the percentage voltage overshoot in SWCNT bundle interconnect over the nominal supply voltage versus bundle width and the width-to-bundle separation ratio when inductive effects are taken into account. Similar to the delay behavior, little or no overshoot occurs when $R \gg \omega L$. However, when inductive effects become significant, voltage overshoot can become a significant issue that must be effectively controlled. Figure 5.6 depicts the absolute difference in percentage voltage overshoot between SWCNT bundle interconnect and
standard copper interconnect over the nominal supply voltage. Since the resistance of SWCNT bundles is typically lower than that of standard copper interconnect, inductive effects impact the performance and reliability of SWCNT bundles with smaller dimensions than standard copper interconnect. Therefore, it is critical that certain steps be taken in the design of SWCNT bundle interconnect systems to reduce the impact of inductive effects [6].

5.1.4 Relative Impact of Magnetic and Kinetic Inductance

Inductive effects such as delay and voltage overshoot typically impact interconnect performance and reliability when the inductive reactance ($\omega L$) is significant compared to the resistance ($R$) in the system's total impedance ($Z = R + j\omega L$) [81]. To determine the impact of kinetic inductance ($L_{kin}$) on SWCNT bundle performance,
we simulated $\omega L_{\text{kin}}/R$ for various interconnect geometries predicted by the 2016 node in [1]. As depicted in Figure 5.7a, $\omega L_{\text{kin}}/R \ll 1$, and therefore, $L_{\text{kin}}$ will have a relatively small impact on inductive effects such as delay and voltage overshoot. Since both $L_{\text{kin}}$ and $R$ are inversely proportional to $N_b$, $\omega L_{\text{kin}}/R$ stays relatively constant and is not impacted by increases in $s_b/w_b$ for a fixed $w_b$.

To quantify the relative impact of magnetic inductance ($L_{\text{mag}}$) and $L_{\text{kin}}$ on the delay and voltage overshoot arising from inductive effects, we performed HSPICE simulations on the RLC model described in Chapter 3 with driver parameters and transistor load capacitances specified by the 2016 node (22 nm technology) in [1]. Figures 5.8a and 5.8b display the percentage difference in delay and voltage overshoot when modeling both the magnetic and kinetic inductances ($L_{\text{tot}}$) and only $L_{\text{mag}}$ versus
$w_b$ and $s_b/w_b$. The addition of $L_{\text{kin}}$ increases the delay by a maximum of 6% and voltage overshoot by a maximum of 3%. Therefore, the $L_{\text{kin}}$ has a relatively small impact even if the worst-case theoretical value is assumed.

To determine what SWCNT bundle geometries and operating conditions will be impacted by $L_{\text{kin}}$, we simulated $\omega L_{\text{kin}}/R$ for various operating frequencies and $d_t$ values as displayed in Figure 5.7b. We assumed a low contact resistance (6.5 kΩ) to maximize the worst-case value of $\omega L_{\text{kin}}/R$. Individual SWCNTs with larger diameters have lower contact and ohmic resistances, which will increase $\omega L_{\text{kin}}/R$. For $L_{\text{kin}}$ to have a large overall impact on SWCNT bundle performance ($\omega L_{\text{mag}}/R \approx 1$), the operating frequency must approach 100 GHz and $d_t$ must be relatively large ($d_t > 2 \text{ nm}$), which increases the overall resistance of SWCNT bundles. Therefore, for configurations where SWCNT bundles offer resistive advantages over copper technology, $L_{\text{kin}}$ will have a small impact on interconnect performance.

5.2 Design of CNT Bundle-Based Interconnect

5.2.1 Optimal CNT Diameter Selection

Given the behavior of resistivity ($\rho_M$) versus $L$ discussed in Section 4.2, determining the cross-over length ($L_{\text{co}}$) between the regimes where the optimal diameter is the smallest or largest feasible diameter is crucial for designing low resistivity nanotube-based interconnect. To calculate $L_{\text{co}}$, we determine the CNT length where
the resistivity of CNT bundles with the largest and smallest feasible outer diameters \((d_{olf} \text{ and } d_{osf})\) and inner diameters \((d_{ilf} \text{ and } d_{isf})\) are equal by solving

\[
\rho_M[R_{ul}, d_{olf}, d_{ilf}] = \rho_M[R_{ts}, d_{osf}, d_{isf}]
\]

(5.1)

for \(L\) where \(\rho_M[R_{ul}, d_{olf}, d_{ilf}]\) and \(\rho_M[R_{ts}, d_{osf}, d_{isf}]\) are the resistivity values for MWCNT bundles calculated using (4.1) with \(d_{out} = d_{olf}\) and \(d_{out} = d_{osf}\), respectively, with \(d_{in} = d_{ilf}\) and \(d_{in} = d_{isf}\), respectively, and with \(R_{tot} = R_{ul}\) and \(R_{tot} = R_{ts}\), respectively.

Since the formulation for \(R_{ul}\) and \(R_{ts}\) in (3.16) and (3.22) depends on the digamma function, a closed-form solution for (5.1) cannot be readily obtained. Therefore, to approximate \(R_{ul}\) and \(R_{ts}\) in (5.1), we solve for the contributions from \(R_o\) and \(R_f\) independently, which is valid since the relative contributions from \(R_o\) and \(R_f\) do not vary substantially between each shell. Based on this approximation,

\[
R_{tot} \approx \frac{1}{\sum_{j=0}^{N} (\frac{C_4(d_{in} + jS)}{R_{qL}})N_c} + \frac{1}{\sum_{j=0}^{N} (\frac{N_c}{R_f})}
\]

(5.2)

Assuming that \(N_c = a(d_{in} + jS) + b\) for \(d_{out} > C_{N_c}\), we expand the summation in (5.2) to obtain the following approximate resistivity formula for an MWCNT with the largest feasible diameter,

\[
\rho_M[R_{ul}, d_{olf}, d_{ilf}] \approx \frac{-\sqrt{3}S_S(A_4 + A_5)(d_{olf} + S_t)^2}{L(d_{ilf} - d_{olf} - S_t)},
\]

(5.3)
where

\[ A_4 = \frac{R_f}{2b + a(d_{uf} + d_{ol})}, \]  

\[ A_5 = \frac{3R_qL}{C_\lambda(3b(d_{uf} + d_{ol}) + aB_1)}, \]  

\[ B_1 = 2d_{uf}^2 + 2d_{uf}d_{ol} + 2d_{ol}^2 - d_{uf}S_s + d_{ol}S_s. \]

Similarly, assuming that \( N_c = 2P_m \) for \( d_{out} < C N_c \), we expand the summation in (5.2) to obtain the following approximate resistivity formula for an MWCNT or SWCNT with the smallest feasible diameter,

\[ \rho_M[R_{uf}, d_{osf}, d_{isf}] \approx -\sqrt{3}S_sA_6(d_{osf} + S_s)^2, \]  

where

\[ A_6 = \frac{2R_qL + C_\lambda(d_{isf} + d_{osf})R_f}{4C_\lambda LP_m(d_{isf} + d_{osf})(d_{isf} - d_{osf} - S_s)}. \]

Substituting (5.3) and (5.7) into (5.1) and solving for \( L \) yields a closed-form expression for \( L_{co} \),

\[ L_{co} = \frac{C_\lambda R_f(A_7 - A_8)(A_9 + A_{10})(d_{isf} + d_{osf})}{2R_q(2b + a(d_{uf} + d_{ol}))A_{11}}, \]

where the terms in the numerator are

\[ A_7 = 4P_m^2P_m(d_{isf} - d_{osf} - S_s), \]
\[ A_8 = (2b + a(d_{lf} + d_{olf}))P_s^2(d_{lf} - d_{olf} - S_s), \quad (5.11) \]

\[ A_9 = 3b(d_{lf} + d_{olf}), \quad (5.12) \]

\[ A_{10} = a(2d_{lf}^2 + d_{lf}(2d_{olf} - S_s) + d_{olf}(2d_{olf} + S_s)), \quad (5.13) \]

and the terms in the denominator are

\[ A_{11} = B_2 + P_s^2(d_{lf} - d_{olf} - S_s)(3b(d_{lf} + d_{olf}) + aB_3), \quad (5.14) \]

\[ B_2 = 6P_t^2P_m(d_{osf}^2 - d_{isf}^2 + S_s(d_{isf} + d_{osf})), \quad (5.15) \]

\[ B_3 = 2(d_{lf}^2 + d_{lf}d_{olf} + d_{olf}^2) + S_s(d_{olf} - d_{lf}) \quad (5.16) \]

where \( P_t = d_{olf} + S_{tt} \), \( P_s = d_{osf} + S_{ts} \), \( S_{tt} \) is the \( S_t \) value for the nanotubes in the large diameter bundle, and \( S_{ts} \) is the \( S_t \) value for the nanotubes in the small diameter bundle. Note that (5.9) can be applied to SWCNT bundles without the loss of generality if \( d_{osf} = d_{isf} \equiv d_t \).

For the case where \( d_{lf} = d_{olf}/2 \) for a typical large diameter MWCNT and \( d_{isf} = d_{osf} \) for an SWCNT, (5.9) is simplified to

\[ L_{co} = \frac{-C_AR_fd_{olf}d_{osf}A_{12}A_{13}}{R_qA_{14}} \quad (5.17) \]

where

\[ A_{12} = 9b + a(7d_{olf} + S_s), \quad (5.18) \]
\[ A_{13} = (P_s^2(4b + 3ad_{of})(d_{of} + 2S_s) - 16P_t^2P_mS_s), \]  
(5.19)

\[ A_{14} = (4b + 3ad_{of})(B_4 + d_{of}P_s^2A_{12}(d_{of} + 2S_s)), \]  
(5.20)

\[ B_4 = -48d_{of}P_t^2P_mS_s. \]  
(5.21)

Similarly, for the case where \( d_{sf} = d_{of}/2 \) for a typical large diameter MWCNT and \( d_{isf} = d_{of}/2 \) for a typical small diameter MWCNT, (5.9) is simplified to

\[ L_{co} = \frac{-3C\lambda R_fd_{of}d_{of}A_{12}(A_{15} - A_{16})}{4R_qA_{14}} \]  
(5.22)

where

\[ A_{15} = (4b + 3ad_{of})P_s^2(d_{of} + 2S_s), \]  
(5.23)

\[ A_{16} = 8P_t^2P_m(d_{of} + 2S_s), \]  
(5.24)

and \( B_4 \) in \( A_{14} \) is

\[ B_4 = -18d_{of}P_t^2P_m(d_{of} + 2S_s). \]  
(5.25)

The less complex formulations for the cross-over length presented in (5.17) and (5.22) can be utilized to determine the optimal nanotube diameter for common nanotube bundle geometries when considering large diameter MWCNTs, small diameter MWCNTs, and SWCNTs.

Based on the simulated MWCNT resistivity results presented in Figure 4.8, the nanotube resistivity decreases as the length increases due to the fixed contact resis-
tance. Therefore, a crossover length also exists between the shorter conductor lengths where copper will have lower resistivity and the longer conductor lengths where CNTs will have lower resistivity. Using the same procedure, we have also developed generalized closed-form expressions for the resistivity cross-over length between large diameter MWCNTs and copper interconnect (by solving $\rho_M[R_{dl}, d_{olf}, d_{ulf}] = \rho_{Cu}$ for $L$) and for the resistivity cross-over length between small diameter MWCNTs/SWCNTs and copper interconnect (by solving $\rho_M[R_{ls}, d_{osf}, d_{isf}] = \rho_{Cu}$ for $L$). For the typical case where $d_{ulf} = d_{ulf}/2$ for a typical large diameter MWCNT, the large diameter MWCNT-copper resistive crossover length is

$$L_{co-cu} = \frac{4\sqrt{3}C_\lambda d_{ulf}P_{l}^2 R_f S_s A_{12}}{(4b + 3ad_{ulf})A_{17}}$$

(5.26)

where

$$A_{17} = C_\lambda d_{ulf} A_{12} \rho_{Cu}(d_{ulf} + 2S_s) - 12\sqrt{3}R_qP_{l}^2 S_s.$$  

(5.27)

For the typical case where $d_{isf} = d_{osf}/2$ for a typical small diameter MWCNT, the small diameter MWCNT-copper resistive crossover length is

$$L_{co-cu} = \frac{3\sqrt{3}C_\lambda d_{osf}P_{s}^2 R_f S_s}{6P_mC_\lambda d_{osf} \rho_{Cu}(d_{osf} + 2S_s) - 4\sqrt{3}R_qP_{s}^2 S_s},$$

(5.28)

and for the SWCNT case where $d_{isf} = d_{osf}$, the SWCNT-copper resistive crossover
Figure 5.9: Comparison of $L_{co}$ predicted using (5.9) and determined using numerical search methods for various $d_{osf}$ and $R_f$ values.

The crossover length is

$$L_{co-cu} = \frac{\sqrt{3}C_\Lambda d_{osf} P_s^2 R_f}{4P_mC_\Lambda d_{osf} \rho_{Cu} - \sqrt{3}R_f P_s^2}.$$  \hspace{1cm} (5.29)

Note that if the resistive cross-over length for a particular type of conductors does not exist for a certain set of process parameters, the formulations for $L_{co}$ and $L_{co-cu}$ will typically produce a negative number.

To verify the accuracy of the developed formulation for $L_{co}$, we compared the $L_{co}$ values calculated using (5.9) with those obtained by numerically searching the design space, and the results of the comparison are displayed in Figure 5.9. We assume that $S_t = 0.34 \text{ nm}$, $d_{in}/d_{out} = 0.5$, and $d_{osf} = 2 \text{ nm}$ or $d_{osf} = 4 \text{ nm}$. The analytical model results closely match the actual crossover length determined using a numerical search algorithm for various maximum $d_{out}$ values. Note that the less complex formulation in (5.22) also matches the results using (5.9) since $d_{in}/d_{out} = 0.5$. For a more extensive
set of simulations with approximately 5000 different combinations of $S_t$, $d_{in}/d_{out}$, and $d_{of}$ values, we found that the average difference between the $L_{\infty}$ values obtained from the proposed analytical formulations and from the numerical search method was 2.5%. The average difference between the $L_{\infty-cu}$ values obtained from the numerical search method and from (5.26), (5.28), and (5.29) for large diameter MWCNTs, small diameter MWCNTs, and SWCNTs was 1.2%, 2.8%, and 0.8%, respectively. Therefore, the analytical formulations for $L_{\infty}$ and $L_{\infty-cu}$ can provide an accurate means for selecting the optimal nanotube diameter in nanotube-based interconnect.

5.2.2 Optimal CNT Bundle Dimension Selection

The conductor height-to-width aspect ratio for standard copper interconnect continues to increase as process technology scales downward in order to provide sufficient current carrying capabilities to minimize electromigration [1]. Since CNTs can reliably handle three orders of magnitude larger current densities than copper interconnect [16], CNT-based interconnect provides the flexibility to utilize interconnect structures with smaller cross-sectional areas than are possible for copper wires due to electromigration constraints. For interconnect in current and future nano-scale process technologies, the coupling capacitance between adjacent conductors typically plays a larger role in determining the wire delay than the ground capacitance. Therefore, we focus on optimizing the height of the nanotube bundles to provide a mechanism to reduce the delay impact of coupling capacitance.
To determine the optimal nanotube bundle dimensions, we employ an analytical delay model to capture the delay impact of nanotube bundle height changes:

\[
\tau = A_{18} R_d (C_d + A_{19} + C_l) + A_{18} R_{tb} \frac{t_{bn}}{t_b} (A_{19} + C_l)
\]  

(5.30)

where

\[ A_{18} \approx 0.69 \quad \text{and} \quad A_{19} = S_f C_{cma} \frac{t_b}{t_{bn}} + S_f C_{cmf} + C_{gs} + C_{gf} \frac{t_b}{t_{bn}}. \]  

(5.31)

\( R_d \) and \( C_d \) are the driver resistance and capacitance, \( C_l \) is the load capacitance, \( C_{cma} \) is the coupling capacitance between the sides of the nanotube bundle and the adjacent conductors, \( C_{cmf} \) is the fringe capacitance between the top of the nanotube bundle and the adjacent conductors, \( C_{gs} \) is the capacitance between the bottom of the nanotube bundle and the conductors/substrate below, \( C_{gf} \) is the fringe capacitance between the sides of the nanotube bundle and the conductors/substrate below, and \( S_f \) is the switch factor for the adjacent conductors [225]. The variable \( t_{bn} \) is the nominal bundle height at which the interconnect parameters \( (R_{tb}, C_{cma}, C_{cmf}, C_{gs}, C_{gf}) \) are extracted based on the model presented in Chapter 3 using the optimal nanotube diameter produced by the design technique presented in Section 5.2.1.

To optimize the nanotube bundle height for minimum delay, we solve \( \frac{d\tau}{dt_b} = 0 \) for \( t_b \), which yields an optimal bundle height of

\[
t_{bo} = \sqrt{\frac{t_{bn}^2 R_{tb} (C_{gs} + S_f C_{cmf} + 2C_l A_{19})}{2 A_{18} R_d (C_{gf} + S_f C_{cma})}}.
\]  

(5.32)

Note that the minimum of the bundle width \( (w_b) \) and \( t_{bo} \) should be used as \( d_{bf} \).
when determining $L_{co}$ in (5.17). Since modifying $d_{olf}$ changes the resistivity of the bundle, we iteratively apply (5.32) by extracting the bundle using the obtained $t_{bo}$ value, plugging in the new extracted values into (5.32), and solving for a new $t_{bo}$ value. This process typically requires a small number of iterations to converge to the optimal $t_{bo}$ value. Using the bundle dimensions specified by (5.32) and the optimal nanotube diameter described in Section 5.2.1, both the capacitance and resistance of MWCNT/SWCNT-based interconnect can be designed to deliver optimal performance.

5.3 Optimal CNT Interconnect Design Results

5.3.1 Performance of Optimized CNT Bundles

To demonstrate the effectiveness of the proposed CNT interconnect design method and to examine the performance of future CNT-based interconnect solutions, we utilize the design method to select the CNT diameter and bundle height to minimize delay for a wide range of length values. We compare the performance of CNT bundles designed using the proposed method to (1) minimum delay bundles with the CNT diameter and bundle height selected using a numerical search method, (2) SWCNT bundles with a 2-to-1 height-to-width aspect ratio and CNT diameters numerically optimized based on the resistance model developed in [38], (3) MWCNT bundles with 2 large diameter MWCNTs to form a 2-to-1 aspect ratio, (4) mono-layer [172], (5) bi-
Figure 5.10: (a) Delay, (d) resistance, and (e) capacitance for several different types of CNT bundles normalized to the delay, resistance, and capacitance of copper conductors in 22 nm technology. Figures (b) and (c) display the optimized bundle height and nanotube diameter for bundles designed using a numerical search for the lowest delay and designed using the proposed method.

layer [175], and (6) quad-layer SWCNT bundles with SWCNT diameters numerically optimized based on the resistance model developed in [38], and (7) scaled copper interconnect. We assume that $w_b = 22 \text{ nm}$ and that the conductors have a maximum aspect ratio of 2-to-1. We utilize driver and load parameters based on the 2016 node in [1]. We assume that $R_f = 20 \text{ k}\Omega$, $P_m = 1/3$, $S_t = 0.34 \text{ nm}$, and $d_{in}/d_{out} = 0.5$ for MWCNTs.

Figure 5.10 displays the delay, resistance, and capacitance for the aforementioned types of CNT bundles normalized to their respective values for copper conductors.
The delay, bundle height, and CNT diameter realized using the proposed method closely match the delay and dimensions of CNT bundles selected using the numerical search method. Therefore, the proposed design method provides an efficient means for determining the optimal CNT diameter and bundle height for a given conductor length. The optimized bundles provide significantly less delay than scaled copper interconnect for the entire range of length values examined with a 29% delay reduction when \( L = 1 \, \mu m \) and a 69% delay reduction when \( L = 1000 \, \mu m \). The proposed design method also decreases delay by 21% and 29% on average compared to non-optimized MWCNT and SWCNT bundles for the range of length values considered.

The optimized bundle height and CNT diameter make this delay reduction possible for local, intermediate, and global interconnect applications. For interconnect in current and future process technologies, the ratio of the driver/load capacitance to the per unit length wire capacitance is smaller than the ratio between the driver resistance and the per unit length wire resistance [172]. Therefore, the wire capacitance has a greater impact on delay than the wire resistance for interconnect with relatively short \( L \) values while wire resistance becomes important for delay for relatively long wire length values, which is evident from (5.30). Therefore, for short wires, the optimized nanotube bundles have smaller height values (Figure 5.10b) to reduce the wire capacitance (Figure 5.10e) at the expense of increased wire resistance (Figure 5.10d). As the wire length increases and resistance becomes more important for reducing delay relative to capacitance, the optimal bundle height increases.
The mono-layer and bi-layer SWCNT bundles proposed in [172] and [175] provide lower capacitance but significantly larger resistance than the optimized CNT bundles. This non-optimal resistance/capacitance combination produces larger delays than the optimized CNT bundles and copper wires for local interconnect applications. Increasing the SWCNT bundle thickness to four layers provides less delay than copper interconnect for local interconnect, but the delay is still significantly higher than the delay achieved by the optimized CNT bundles. Note that the delay advantages of mono-layer, bi-layer, and quad-layer SWCNT bundles for local interconnect will be heavily dependent on the driver resistance and load capacitance. In contrast, the proposed design method provides the flexibility to determine the optimal CNT bundle height for an arbitrary set of driver and load parameters.

5.3.2 Fabrication Requirements for Optimized CNT Bundles

For CNT bundles to be an attractive interconnect solution, CNT-based interconnect must not only reliably achieve greater performance than scaled copper interconnect but also must have a cost-effective means of fabrication in future nano-scale ICs. One of the major limitations currently facing CVD-based nanotube bundle fabrication techniques is the relatively low density of nanotubes realized in a bundle as discussed in Section 2.3. Given the large range of possible nanotube diameters for interconnect applications, the percentage area covered by CNTs ($P_A$) provides a better metric than the nanotube density for evaluating the effectiveness of CNT fabrication.
Figure 5.11: Required spacing between nanotubes in a bundle versus $P_A$ for $d_{out}$ values of 1, 2, 5, 10, 20, 50, and 100 nm. The experimentally realized result displayed in the figure reflects the nanotube density achieved by the vertical CNT bundles in [2,3].

Techniques for producing low resistance bundles. For a hexagonal unit cell in a CNT bundle, the percentage area covered by CNTs is

$$P_A = \frac{\text{CNT Area}}{\text{Total Area}} = \frac{100\pi d_{out}^2}{2\sqrt{3}(d_{out} + S_t)^2},$$

which yields an $S_t$ value for a given $P_A$ of

$$S_t[P_A] = \frac{3^{3/4}d_{out}}{6} \sqrt{\frac{200\pi}{P_A}} - d_{out}.$$  

Figure 5.11 displays the required $S_t$ value needed to achieve a given $P_A$ value for various $d_{out}$ values. Smaller diameter CNTs require lower $S_t$ values to achieve a given $P_A$ value.
Figure 5.12: CNT-Cu delay upper and lower cross-over lengths for CNT bundles both with and without optimized heights for the different technology nodes in the ITRS roadmap [1] for the following maximum CNT area coverage values ($P_A$): (a) 5%, (b) 7.5%, (c) 10%, (d) 15%, (e) 20%, and (f) 25%. The lightly shaded areas denote the length values where CNT bundles with optimized height have less delay than copper interconnect, and the darkly shaded areas denote the length values where CNT bundles both with and without optimized height have less delay than copper interconnect.

To determine the $P_A$ values in the CNT fabrication process required to make nanotube-based interconnect a competitive solution compared to scaled copper wires in terms of delay, we simulated (a) CNT bundles with optimized height and optimized CNT diameter and (b) bundles with a 2-to-1 aspect height-to-width ratio and optimized CNT diameter for a large range of $L$ values in various ITRS technology nodes [1]. Figure 5.12 displays the upper and lower cross-over length values where CNT bundle delay and copper delay are equal for maximum CNT area coverage ranging from 5% to 25%. In terms of the interconnect delay, three general cases for a given $P_A$ value are possible: (1) the CNT bundle delay values are greater than those of copper interconnect for all $L$ values, (2) the CNT bundle delay is less than the
copper wire delay for a set of $L$ values with both upper and lower bounds, and (3) the CNT bundle delay is less than the copper wire delay for a set of $L$ values with only a lower bound.

In the first case, the low $P_A$ value raises the resistance of the CNT bundle to a level where the delay of the copper interconnect will always be less than the delay of the bundle in spite of the reduced capacitance provided by height optimization. In these cases, the normalized delay profile versus $L$ is similar in shape to the mono-layer or bi-layer SWCNT bundle delay displayed in Figure 5.10. When an upper cross-over length exists (case 2), the resistance of the bundle is greater than the copper wire resistance for all length values, but the optimized height reduces the capacitance of the bundle for short and intermediate $L$ values. In these cases, the normalized delay profile versus $L$ is similar in shape to the quad-layer SWCNT bundle delay displayed in Figure 5.10. When no upper cross-over length exists (case 3), the resistance of the bundle is less than the copper wire resistance when $L$ is larger than a certain value, which makes the delay of the CNT bundle less than the copper wire delay for interconnect longer than a certain length. In these cases, the normalized delay profile versus $L$ is similar in shape to the optimized bundle delay displayed in Figure 5.10.

The $P_A$ achieved by future CNT bundle fabrication processes will greatly determine the performance of CNT-based interconnect solutions. $P_A$ must be at least 15% for height optimized CNT bundles to provide less delay than copper interconnect for a certain range of $L$ values in all ITRS technology nodes, and for CNT bundles with-
out height optimization, $P_A$ must be at least 25% to achieve lower delay than copper interconnect for the same conditions. Therefore, in general, CNT bundle height optimization reduces the required $P_A$ necessary to achieve a given level of performance by 5% to 10% compared to CNT bundles without height optimization. To achieve superior performance to copper interconnect for all technology nodes and for all length values above 1 $\mu m$, $P_A$ must be at least 30% for height optimized CNT bundles, $P_A$ must be at least 35% for MWCNT bundles without height optimization but with diameter optimization, and $P_A$ must be at least 40% for SWCNT bundles without height optimization.
Chapter 6

Implications of Process Variations for Carbon Nanotube Interconnect

As process technology continues to scale downward and physical interconnect dimensions become smaller, the impact of process variations on interconnect characteristics is becoming increasingly significant. For standard copper interconnect, multi-conductor pattern erosion and dishing within individual conductors due to chemical-mechanical polishing can have a significant impact on conductor thickness, and conductor line width may also vary due to subwavelength lithographic distortions [1,226]. Given the manufacturing challenges associated with future nanotube-based interconnect, investigating the impact of the process variations associated with SWCNT bundles and comparing these sources of variation to those in scaled copper interconnect is vital for evaluating the reliability of future nanotube-based interconnect solutions.
In this chapter, we investigate the impact of process variations on future CNT-based interconnect solutions. We examine the impact of variations for nanotube-based interconnect structures consisting of SWCNT bundles and large diameter MWCNTs. These structures are predicted to provide the optimal interconnect delay for local and global interconnect applications based on the results presented in Section 5.3.

6.1 Sources of Variation for SWCNT Bundles

For future interconnect solutions based on SWCNT bundles, we have identified 10 possible sources of manufacturing variation, which are depicted in Figure 6.1. The sources of variation include (a) the probability that a given nanotube is metallic; (b) inter-bundle variation in the spacing between individual nanotubes; (c) intra-bundle variation in individual nanotube diameter; (d) inter-bundle variation in average individual nanotube diameter; (e) intra-bundle variation in contact resistance for individual nanotubes; (f) inter-bundle variation in average contact resistance; (g) intra-bundle variation in mean free path of acoustic and optical phonon scattering effecting both $\lambda_{ap}$ and $I_o$; (h) variation in dielectric thickness between interconnect layers of nanotube bundles; (i) variation in bundle width values; and (j) variation in bundle height values. Note that the last three listed sources of variation [(h)-(j)] are also present for standard copper interconnect in scaled process technologies.

One of the most critical challenges to realizing high performance SWCNT-based interconnect is controlling the proportion of metallic nanotubes in the bundle. SWCNT
Figure 6.1: Sources of variation in SWCNT bundle interconnect include (a) the probability that a given nanotube is metallic; (b) inter-bundle variation in the spacing between individual nanotubes; (c) intra-bundle variation in individual nanotube diameter; (d) inter-bundle variation in average individual nanotube diameter; (e) intra-bundle variation in contact resistance for individual nanotubes; (f) inter-bundle variation in average contact resistance; (g) variation in mean free path of acoustic and optical phonon scattering effecting both $\lambda_{ap}$ and $I_o$; (h) variation in dielectric thickness between interconnect layers; (i) variation in bundle width values; and (j) variation in bundle height values.
Correlation of $d_t$ Within Bundle

<table>
<thead>
<tr>
<th>Correlation of $d_t$ Within Bundle</th>
<th>Percentage 3σ $d_t$ Variation</th>
<th>Percentage 3σ Delay Variation with Other Variation Sources</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Intra-Bundle</td>
<td>Inter-Bundle</td>
</tr>
<tr>
<td>1.00</td>
<td>50.00</td>
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</tr>
<tr>
<td>0.81</td>
<td>48.72</td>
<td>15.81</td>
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<tr>
<td>0.64</td>
<td>44.18</td>
<td>22.36</td>
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<td>0.49</td>
<td>41.17</td>
<td>27.39</td>
</tr>
<tr>
<td>0.36</td>
<td>38.10</td>
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<td>35.34</td>
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<tr>
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<td>30.77</td>
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<td>28.01</td>
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<td>22.19</td>
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<td>15.73</td>
<td>47.42</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>50.00</td>
</tr>
</tbody>
</table>

Table 6.1: 3σ percentage delay variation when certain sources of SWCNT bundle variations are present for a given level of $d_t$ correlation within the bundle.

Bundles have metallic nanotubes that are randomly distributed within the bundle with probability $P_m = 1/3$ if no special metallic nanotube separation techniques are utilized [97]. $P_m$ may cause reliability problems in SWCNT bundle interconnect since $N_b$ decreases as the cross-sectional dimensions of the bundle are reduced.

For certain SWCNT-specific sources of variation such as $d_t$ variation, the type of variation can be classified as *intra-bundle*, where a given distribution exists for a certain parameter associated with the individual SWCNTs within a given bundle, or classified as *inter-bundle*, where a given distribution exists for the mean values of a certain parameter in a set of bundles. The level of inter-bundle and intra-bundle variation depends on the correlation between the values of a particular parameter for the SWCNTs within a bundle. For instance, if the $d_t$ values for the SWCNTs within a given bundle are strongly correlated, then the inter-bundle $d_t$ variation will be close to the standard deviation of the overall SWCNT $d_t$ distribution in a large-scale sample with many bundles. In this case, the intra-bundle $d_t$ variation will be significantly
smaller than the overall SWCNT $d_t$ variation in the sample. In contrast, if the SWCNT diameters within a given bundle are weakly correlated, then the intra-bundle $d_t$ variation will be significantly larger than the inter-bundle $d_t$ variation. The inter-bundle and intra-bundle $d_t$ variations associated with various correlation coefficients for SWCNT diameters within a given bundle are listed in Table 6.1 assuming that the overall $d_t$ distribution has $3\sigma = 50\%$ variation [123,124].

Previous studies have experimentally demonstrated that the bundles that naturally form in common SWCNT synthesis processes have SWCNT diameters that are strongly correlated. In [120,121], the diameters and chiralities of SWCNTs in individual bundles that form in the three different standard synthesis methods discussed in Section 2.3 were measured using electron diffraction and high-resolution transmission electron microscopy. Only small differences in SWCNT diameter and chirality were observed in bundles produced by CVD while the overall variation of SWCNT diameter and chirality for the entire sample was significantly larger. Therefore, the individual SWCNTs within a given bundle may be strongly correlated in certain potential future fabrication processes for SWCNT-based interconnect, which results in large inter-bundle diameter variations with a distribution close to the diameter distribution of the larger SWCNT samples.

We assume that the inter-bundle distribution of SWCNT diameters has a $3\sigma = 50\%$ variation based on the overall $d_t$ distribution described in [123,124]. Note that this assumption provides less optimistic results that those produced by ignoring the
SWCNT diameter correlation within the bundles. Since the spacing between nanotubes is predicted to be closely related to the nanotube diameter [227], we also assume that the SWCNT bundles have an inter-bundle spacing variation of $3\sigma = 23\%$ based on the differences in the $S_t$ values reported in [108,120,121] where $S_t$ ranges from $3.15 \text{ Å}$ to $3.4 \text{ Å}$. However, we do not model the correlation between $d_t$ and $S_t$ or between other sources of variations within a bundle in general due to the computational complexity of correlation modeling for CNT-bundles with a large number of nanotubes and the due to the lack of experimental and theoretical research on the statistical correlations between many of the possible variation sources in SWCNT bundles.

Defects in the chiral structure of metallic carbon nanotubes can significantly alter the mean free path of both acoustic-phonons ($\lambda_{ap}$) in the low bias voltage regime ($V < 0.1V$) and optical-phonons ($\lambda_{op}$) in the high bias voltage regime, which can impact the saturation current of the individual nanotubes ($I_0$) [171]. These defects can cause uncertainty in the ohmic ($R_o$) and high bias ($R_{hb}$) resistances of the individual SWCNTs in the bundle. Variations in the resistance due to imperfect metal-SWCNT contacts ($R_c$) can be caused by statistical uncertainty in the quality of the overall nanotube bundle-metal contact or uncertainty in the quality of contacts between each individual nanotube in the bundle. Since detailed information on the statistical distribution of ohmic and contact resistances has not appeared in the experimental literature, we assume that variations in $\lambda_{ap}$, $I_0$, and $R_c$ have the same $3\sigma$ values as
the reported diameter distribution, 50%, since the nanotube diameter and the ohmic, contact, and high bias resistances are related as discussed in Chapter 3.

Variations in bundle width, height, and dielectric thickness \( h_g \) can impact the resistance, capacitance, inductance, and delay of nanotube bundle-based interconnect. Unlike the aforementioned sources of variation, variations in conductor dimensions also impact standard copper interconnect in scaled process technologies. Multi-conductor pattern erosion and dishing within individual conductors due to chemical-mechanical polishing (CMP) can have a large impact on conductor thickness with 3-sigma variations of up to 35% for future process technologies [1, 228]. Dielectric thickness variations can also result due to the CMP process. Variations in conductor width can occur due to lithographic errors [226]. For SWCNT bundles, the percentage variation in bundle dimensions has not been experimentally investigated in the literature. Therefore, we assume that the percentage variation in bundle dimensions is equivalent to the predicted values for copper interconnect in [1]. Variations in bundle dimensions must be controlled more precisely in future SWCNT based interconnect than they are in standard copper interconnect to achieve the same overall percentage variation in resistance, capacitance, inductance, and delay since SWCNT-based interconnect will also be affected by the aforementioned sources of variation in the individual nanotube characteristics.
6.2 Simulation of Process Variations

To identify the relative importance of each possible source of variation on future nanotube-based interconnect solutions, we have performed an extensive set of Monte Carlo simulations using the circuit model described in Chapter 3 to analyze the impact of each variation on resistance, capacitance, kinetic inductance, magnetic inductance, and delay. Note that do not simulate process variations in driver parameters to highlight the relative impact of process variations on SWCNT bundles and copper interconnect. When possible, we have utilized sources in the literature to determine the expected standard deviation of each type of variation, which is listed in Table 6.2 and described in the preceding section.

For sources of variation that vary inter-bundle [(b), (d), (f), (h) - (j) in Figure 6.1], we determine the mean and standard deviation of the SWCNT interconnect properties from a large number of simulated bundle geometries. We assume that the inter-bundle

<table>
<thead>
<tr>
<th>Variation type</th>
<th>Geometric variation</th>
<th>$3\sigma$ variation percentage in interconnect characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_n$</td>
<td>$P_n = 1/3$</td>
<td>$R_{tot}$</td>
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<tr>
<td>Inter-bundle $S_t$</td>
<td>$3\sigma = 23%$</td>
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<td>Intra-bundle $d_t$</td>
<td>$3\sigma = 4.4%$</td>
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<td>Inter-bundle $d_t$</td>
<td>$3\sigma = 50%$</td>
<td>0.24</td>
</tr>
<tr>
<td>Intra-bundle $R_c$ - Global</td>
<td>$3\sigma = 60%$</td>
<td>32.33</td>
</tr>
<tr>
<td>Intra-bundle $R_c$ - Local</td>
<td>$3\sigma = 60%$</td>
<td>0.03</td>
</tr>
<tr>
<td>Inter-bundle $R_c$ - Global</td>
<td>$3\sigma = 50%$</td>
<td>0.06</td>
</tr>
<tr>
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</tr>
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</tr>
<tr>
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<tr>
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</table>

Table 6.2: Predicted variations in SWCNT bundle process parameters, resistance ($R_{tot}$), capacitance ($C_{cb} + C_{gb}$), kinetic inductance ($L_{kb}$), magnetic inductance ($L_{mb}$), and delay.
process parameter variations are normally distributed since reported experimental
inter-bundle $d_t$ values have this distribution [123,124,227]. To capture the relationship
between the process parameters, we apply each source variation in a hierarchical
manner. For each statistical sample in the Monte Carlo simulation, we first determine
the inter-bundle $w_b$, $t_b$, $h_g$, $d_t$, $S_t$, and $R_c$ values from their respective distributions.
This sets the $N_b$ value for the sampled nanotube bundle interconnect. We then apply
the probability distributions for the intra-bundle sources of variation [(a), (c), (e), (g)
in Figure 6.1] to each individual nanotube in the bundle for each of the sample bundle
geometries in the Monte Carlo simulation. With the exception of $P_m$, we assume that
the intra-bundle variations are also normally distributed. When simulating both
inter and intra-bundle variations, we assume that the sampled inter-bundle value is
the mean for the intra-bundle distribution.

6.3 Impact of Variations on SWCNT Bundles

Table 6.2 displays the 3-sigma variation in SWCNT bundle RLC characteristics
and propagation delay for each of the ten potential sources of process variation. We
utilize the process parameters from the 2016 node of [1] (22 nm technology) and as­
sume a 22 nm bundle width. The SWCNT bundles are .1 mm long unless specified
as local interconnect, in which case the bundles are 10 $\mu$m long. We assume that the
SWCNT have optimal $d_t$ values to minimize the resistance due to the trade-off be­
tween $R_{ob}$ and $R_{cb}$ as discussed in Section 4.1. In 22 nm technology, the inter-bundle
Figure 6.2: Percentage 3-sigma delay variation versus $P_m$ and $w_b$ for inter-bundle sources of variation including (a) variation in average individual nanotube diameter; (b) variation in bundle width values; (c) variation in bundle height values; (d) variation in dielectric thickness between interconnect layers of nanotube bundles; and (e) variation in the spacing between individual nanotubes.

Sources of variation have a significantly larger impact than the intra-bundle variation in nanotube characteristics with the exception of variations due to $P_m$. Inter-bundle variations that effect $N_b$ have a large impact on the resistance and kinetic inductance of the nanotube bundle. Note that while the resistance plays a large role in determining the delay of the bundle, the kinetic inductance has a much smaller role despite its large nominal value since $R \gg \omega L_k$ for the simulated nanotube bundle geometries as discussed in Section 5.1. Variations in magnetic inductance are relatively small since it primarily depends on the overall current loop and has only a second order dependence on conductor dimensions [79]. Only variations in bundle dimensions cause significant statistical variation in capacitance since the capacitance
is primarily determined by the spacing between the bundles and the total surface area of the bundle.

Figure 6.2 displays the percentage 3-sigma delay variation versus $P_m$ and $w_b$ for inter-bundle sources of variation. As $w_b$ decreases, the percentage 3-sigma delay variation increases since the resistance of the bundle increases with respect to the driver resistance. The same trend exists as $P_m$ decreases since the overall resistance of the bundle is increasing relative to the driver resistance and bundle capacitance. Inter-bundle variation in $d_t$ is the most significant source of variation for nanotube bundles since it greatly impacts $N_b$ [39]. Variations in $w_b$ and $h_b$ have a large effect (up to 30% 3-sigma variation in delay) since both the resistance and capacitance of the nanotube bundle are impacted. Variation in $S_t$ has a smaller effect (up to 8% 3-sigma variation in delay) since the experimentally observed 3-sigma variation in $S_t$ is less than the 3-sigma variation in the other inter-bundle sources of process variation.

In general, intra-bundle sources of variation have a relatively small impact on SWCNT bundle delay since they vary for each nanotube in the bundle and the bundle typically contains a large number of nanotubes. Since the impact of intra-bundle sources of variation is dependent on $N_b$, they will become more significant as process technology scales and as the conductor's cross-sectional area decreases. Figure 6.3 displays the percentage 3-sigma delay variation versus $N_b$ for several sources of intra-bundle variation. Intra-bundle variations in $d_t$, $\lambda_{ap}$, $I_o$, and $R_c$ for both local and global interconnect applications cause less than 10% 3-sigma variation in delay for
Figure 6.3: Percentage 3-sigma delay variation versus $N_b$ for several sources of intra-bundle process variation.

2020 node in [1] ($w_b = 14 \text{ nm}$). Therefore, these sources of variation will be relatively insignificant for nanotube bundles with the predicted interconnect dimension in future process technologies. In contrast, delay variation due to $P_m$ can be large with up to 30% 3-sigma variation possible for the interconnect geometries predicted by ITRS assuming $P_m = 1/3$. $P_m$ causes significantly more variation since a given nanotube either has metallic conduction properties or does not contribute to the conduction. This results in a large effective variation in the resistance of the individual nanotubes.

To investigate the impact of $d_t$ correlation within a given bundle, we examine the delay variations for SWCNT bundles with $L = 12.5 \text{ \mu m}$ for different $d_t$ correlation coefficients combined with either (a) no other sources of variation; (b) inter-bundle $S_t$ variation that is scaled proportionally to the level of inter-bundle $d_t$ variation; (c) inter-bundle $S_t$ variation that has a constant standard deviation; (d) all of the
CNT-specific sources of variation depicted in Figure 6.1, which excludes variations in bundle dimensions and dielectric thickness; and (e) all sources of variation depicted in Figure 6.1. The delay variation results are displayed in Table 6.1. In general, a higher degree of $d_t$ correlation within a bundle results in larger delay variations. When only $d_t$ variations are present, the $3\sigma$ delay variation ranges from 1.23% to 4.86%, and the $3\sigma$ delay variation ranges from 20.31% to 21.42% when all sources of variation are present. Therefore, a large $d_t$ correlation within a bundle typically provides a modest increase in overall delay variation. While manufacturing techniques for the efficient IC integration of CNT-based interconnect solutions are still in the investigation phase of their development and specific fabrication methods have not been firmly established, the process variation analysis presented in this section provides a general framework for evaluating the impact of the potential sources of process variation for SWCNT-based interconnect.

6.4 Relative Impact of Process Variations: SWCNT Bundle and Copper Interconnect

To effectively determine the suitability of SWCNT bundles as a replacement for copper interconnect, we must analyze the relative impact of process variations on nanotube-based interconnect solutions and scaled copper interconnect in future process technologies. Since SWCNT bundles will suffer from sources of process variation
that are inherently present in the nanotubes, nanotube-based interconnect will typically experience greater overall variation in resistance, capacitance, and delay than scaled copper interconnect assuming that the percentage variation in conductor dimensions for both technologies is equivalent. Therefore, additional control over conductor dimensions in SWCNT bundles will be required to achieve the same level of variation that is predicted for scaled copper interconnect. This is crucial for ensuring that SWCNT bundle interconnect has the same level of reliability as scaled copper interconnect with respect to process variation in future process technologies.
6.4.1 Impact of All Sources of Process Variations

Figure 6.4 displays the 3-sigma percentage variation in resistance, capacitance, and delay versus the ITRS technology year for SWCNT bundles and standard copper interconnect for both global and local interconnect applications. The difference in resistance variation between SWCNT bundles and copper interconnect is significantly larger than it is for capacitance since the nanotube-specific sources of variation primarily impact resistance. In both the local and global interconnect cases, the interconnect resistance is becoming larger relative to the driver resistance as technology scales. This accounts for the overall increase in delay variation as process technology scales. In the more near-term current nodes of the ITRS roadmap, the percentage difference in 3-sigma delay variation between SWCNT bundles and copper interconnect stays relatively constant since inter-bundle sources of variation, which do not depend on the bundle dimensions, dominate the intra-bundle sources of variation as described in Section 6.3. In the long-term ITRS nodes, the differences between SWCNT bundle and copper interconnect variations increases since $N_b$ becomes small as the bundle dimensions scale, which increases its impact for SWCNT bundle interconnect.

For the local interconnect cases simulated in Figure 6.4, the percentage variation in delay for SWCNT bundles is larger than that of scaled copper interconnect. However, decreasing the SWCNT bundle resistance due to changes in $P_m$ can result in cases where the delay variation of SWCNT-based solutions is less than that of copper interconnect. For instance, if $P_m$ is increased from 1/3 to 0.6, the absolute difference
Figure 6.5: Behavior of 3-sigma percentage variation in delay versus the ITRS technology node and the 3-sigma percentage variation in bundle dimensions for the following cases: (a) global SWCNT bundle interconnect; (b) global copper interconnect; (c) difference between delay variation in global SWCNT bundles and copper interconnect; (d) local SWCNT bundle interconnect; (e) local copper interconnect; and (f) difference between delay variation in local SWCNT bundles and copper interconnect.

In the 3-sigma percentage variation in delay between SWCNT bundles and copper interconnect in the 2016 node of ITRS changes from 5% to -2%. If $P_m$ is increased to 0.9, then the absolute difference in the 3-sigma percentage variation in delay between SWCNT bundles and copper interconnect becomes -5%. Consequently, copper interconnect can have greater delay variation than SWCNT bundles when the mean resistance value for SWCNT bundles is significantly lower than it is for scaled copper interconnect relative to the driver resistance.
6.4.2 Required Control of SWCNT Bundle Dimensions

To achieve the same level of delay variation as scaled copper interconnect, the sources of variation in SWCNT bundles must be effectively controlled. While controlling the nanotube-specific properties of SWCNT bundles could provide one mechanism to reduce the impact of process variations, achieving greater control over the individual nanotube properties during the SWCNT bundle fabrication process remains a difficult challenge [119, 120, 229–231]. Therefore, controlling the variation in the dimensions of the nanotube bundles will probably provide a feasible means for reducing the impact of process variations on nanotube characteristics. Figure 6.5 depicts the behavior of the 3-sigma percentage delay variation versus the 3-sigma percentage variation in bundle dimensions, including dielectric thickness, for both global and local interconnect applications in future process technology. As expected, reducing the percentage variation in bundle dimensions decreases the overall variation in delay for both global and local interconnect as depicted in Figures 6.5a and 6.5d. Furthermore, the trend of larger percentage variations as process technology scales, which was discussed in Section 6.4.1, exists for both SWCNT bundles and copper interconnect as displayed in Figures 6.5a, 6.5b, 6.5d, and 6.5e.

Figures 6.5c and 6.5f depict the percentage difference in delay variation between SWCNT bundles and copper interconnect for both local and global interconnect applications for different values of bundle dimension variation. Note that the ITRS predicted percentage 3-sigma variation in conductor dimensions increases from 30%.
to 35% from the 2010 to 2018 nodes and then decreases slightly to 33% in the 2019 and 2020 nodes [1]. As process technology scales, the decrease in percentage bundle dimension variation needed to make SWCNT and copper interconnect delay variation equivalent remains relatively constant until the 2018 node in ITRS. For these technologies, the absolute reduction in bundle dimension variation required for global interconnect is approximately 12%, which is a 40% relative reduction in conductor dimension variation between SWCNT bundle and copper interconnect. For local interconnect, the required absolute reduction in bundle dimension variation increases due to the increased impact of inter-bundle contact resistance variations to approximately 19%, which is a 63% relative reduction in conductor dimension variation. Beyond the 2018 node, the required absolute reduction in bundle dimension variation increases for both global and local interconnect due to the increasing impact of intra-bundle variations in resistance due to $P_m$.

While controlling the variation in the dimensions of the nanotube bundles will probably provide a feasible means for reducing the impact of process variations on nanotube characteristics, reducing the impact of all sources of variation in SWCNT bundle interconnect could also potentially allow SWCNT bundles to achieve the same level of delay variation as scaled copper interconnect. In Figure 6.6, we display the 3-sigma percentage variation in delay versus the ITRS technology node and the relative percentage variation in the SWCNT bundle process parameters with respect to their nominal predicted 3-sigma variation values listed in Table 6.2. As depicted
Figure 6.6: Behavior of 3-sigma percentage variation in delay versus the ITRS technology node and the relative percentage variation in the SWCNT bundle process parameters with respect to their nominal predicted 3-sigma variation values listed in Table 6.2 for the following cases: (a) global SWCNT bundle interconnect; (b) difference between delay variation in global SWCNT bundles and copper interconnect; (c) local SWCNT bundle interconnect; and (d) difference between delay variation in local SWCNT bundles and copper interconnect.
in Figures 6.6a and 6.6c for global and local SWCNT interconnect, the same general aforementioned trends exist: (1) increasing percentage 3-sigma variation in delay as technology scales; (2) greater variation in global interconnect than in local interconnect due to the larger relative impact of driver resistance for short interconnect length values; and (3) less 3-sigma variation in delay as the variation in the process parameters decreases.

Figures 6.6b and 6.6d depict the absolute difference in delay variation for SWCNT bundles and copper wires in global and local interconnect applications. Note that we utilize the 3-sigma percentage variation displayed in Figures 6.5b and 6.5e when calculating the absolute difference in delay variation. For both global and local interconnect, the percentage decrease in nominal 3-sigma process variation needed to achieve the same level of delay variation in SWCNT and copper interconnect ranges from 10% to 20%. A slightly greater percentage decrease in nominal 3-sigma process variation (≈ 5%) is required to offset the additional variation of SWCNT bundles in global interconnect as process technology scales since intra-bundle sources of variation become more significant in the later technology nodes of the ITRS roadmap. Based on the results displayed in Figures 6.5 and 6.6, controlling the impact of process variations for SWCNT bundles is crucial for ensuring that nanotube-based interconnect has a similar level of reliability as scaled copper interconnect with respect to process variation in future technologies.
Figure 6.7: Percentage variation \((\sigma/\mu)\) in resistance due to the statistical probability that a MWCNT conducting shell/SWCNT is metallic. The insets depict the distribution of resistance values for large diameter MWCNT bundles with \(d_{in}/d_{out} = 0.5\) and \(w_b\) values of 30 nm and 10 nm.

6.5 Impact of Variations on MWCNT Bundles

In the previous sections, we demonstrated that nanotube-specific sources of variation, particularly variation due to \(P_m\), inter-bundle \(d_t\) variation, and inter-bundle \(S_t\) variation, can increase the resistance and delay variation associated with SWCNT bundles. For large diameter MWCNT bundles, the significant nanotube-specific sources of process variation include variation due to \(P_m\), variation in \(d_{out}\), and variation in \(d_{in}\). In this section, we evaluate the impact of nanotube-specific variations on interconnect realized using large diameter MWCNTs, which as we have discussed in Chapter 5, can provide optimal delay performance for global interconnect.

Figure 6.7 depicts the percentage variation \((\sigma/\mu)\) in resistance due to \(P_m\). We capture the resistance probability distributions using Monte Carlo simulations and
assume that $R_f = 20\, k\Omega$, $P_m = 1/3$, $S_t = 0.34\, nm$, and $L = 100\, \mu m$ and that the MWCNT bundles consist of 2 MWCNTs stacked to provide a 2-to-1 height-to-width aspect ratio while the SWCNT bundles have $d_t$ values of 1 nm. This represents the two extreme cases for nanotube diameter in a CNT bundle. We consider full range of experimentally reported inner-to-outer diameter ratios ($d_{in}/d_{out} = 0.80$ to $d_{in}/d_{out} = 0.35$) for the conducting shells in an MWCNT [2,40]. Note that we do not consider variations in bundle dimensions and dielectric thickness since these sources of variation will likely be common to both SWCNT and MWCNT bundles and have already been investigated in the previous sections.

Based on Figure 6.7, large diameter MWCNT bundles experience significantly larger resistances variations due to $P_m$ than SWCNT bundles since the number of conducting shells in a large diameter MWCNT bundle is significantly less than the number of nanotubes in an SWCNT bundle. For instance, for a bundle width of 10 nm, the MWCNT bundle with 2 stacked nanotubes only contains 14 conducting shells, while the SWCNT bundle contains 128 nanotubes. Therefore, the variation due to $P_m$ is more greatly averaged out for SWCNT bundles than it is for large diameter MWCNT bundles. Furthermore, as the bundle width decreases, the CNT diameter in a maximum diameter MWCNT bundle decreases, which causes the number of conduction channels provided by the semiconducting shells in the MWCNT to decrease relative to the number of conduction channels provided by the metallic shells. This further increases the resistance variation due to $P_m$ for large diameter
MWCNT bundles as the bundle width decreases. Also, the increase in semiconducting shell resistance for the smaller MWCNT diameter values in bundles with smaller width values causes the distribution of MWCNT bundle resistance values to become increasingly skewed to the right with the distribution of resistance values closely approximating a lognormal distribution when \( w_b = 10 \, nm \).

To assess the level of resistance variation for large diameter MWCNT bundles due to the other sources of nanotube-specific process variations, we simulated the mean resistance, the resistance at which there is a 95% probability of obtaining a larger resistance (lower 95%), and the resistance at which there is a 95% probability of obtaining a smaller resistance (upper 95%). The results are presented in Table 6.3.
Figure 6.8: Probability of a timing failure for (a) large diameter MWCNT bundles and (b) SWCNT bundles for various bundle widths and levels of timing slack. Figure (c) shows the difference in timing failure probability between large diameter MWCNT bundles and SWCNT bundles.

where the reported values are normalized to the nominal resistance calculated using the resistance model presented in Section 3.2. We assume that $P_m = 1/3$ and that $d_{out}$ and $d_{in}$ are normally distributed with $3\sigma = 50\%$.

Based on the results presented in Table 6.3, $P_m$ is the most important source of variation for MWCNT bundles, but variations in $d_{out}$ and to a lesser extent in $d_{in}$ are also significant. However, even the variation due to $d_{in}$ is larger than the variation of any given individual variation source for SWCNT bundles. Also, note that the mean resistance does not equal the nominal resistance for the MWCNT bundle cases due to the lognormal nature of the resistance distributions. For the combined impact of all nanotube-specific sources of variation, the upper 95% bound for the resistance probability for large diameter MWCNT bundles is an order of magnitude larger than it is for SWCNT bundles.

To compare the timing implications of the resistance variation associated with large diameter MWCNT bundles and SWCNT bundles, we simulated the probability of a timing failure for the MWCNT and SWCNT bundles, which is depicted in

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Figure 6.8. SWCNT bundles provide relatively robust behavior with a timing slack of 7% to 37% percent required for bundles width values ranging from 50 nm to 10 nm to achieve a 1% timing failure probability. In contrast, large diameter MWCNT bundles are significantly less reliable due to their large resistance variation. For the timing failure probability to reach 1% for large diameter MWCNT bundles, the timing slack must be 109% for a bundle width of 50 nm and 1260% for a bundle width of 10 nm, which is most likely unacceptable for interconnect applications in future nano-scale ICs. Therefore, to reliably utilize large diameter MWCNT bundles for nanotube-based interconnect, the nanotube diameter variation must be significantly reduced and the variation due to $P_m$ must be reduced by enlarging $P_m$. Alternatively, MWCNTs must be designed utilizing smaller $d_{oil}$ values when determining the optimal nanotube diameters based on $L_{co}$ as discussed in Section 5.2 in order to realize reliable and low resistance global interconnect.
Chapter 7

Carbon Nanotube-Based

Integrated Inductors

For analog and mixed-signal VLSI applications, integrated inductors continue to limit the performance of mixed-signal systems [22,232]. Numerous analog circuits such as low noise amplifiers (LNA) [21,22,56–77], voltage controlled oscillators [17], and RF filters [19,20,78] depend on low loss integrated inductors. Integrated inductors suffer from complex loss mechanisms in the metal and substrate, and consume large chip area, making them difficult to characterize and expensive to implement. Resistive losses in the inductor’s conductors are increased at high frequencies due to non-uniform current distribution resulting from skin and proximity effects [64]. To improve the performance of integrated inductors for future mixed-signal systems, alternative technologies must be investigated.
In this chapter, we propose low loss on-chip inductors leveraging SWCNT bundles. Although we focus on SWCNT bundle-based inductors in this chapter, MWCNT bundle-based inductors can provide similar performance advantages based on the resistance results presented in Chapter 4. We develop a model for high frequency current re-distribution in SWCNT bundles, which we find can have a large effect on the resistance and quality factor of nanotube-based inductors. We then examine the potential quality factor improvement provided by nanotube-based inductors over copper-based inductors for mixed-signal circuit applications. The results indicate that optimized SWCNT bundle-based inductors can provide a significant quality factor increase over copper-based inductors, which can provide a significant noise figure and power consumption improvement in optimized narrow-band LNAs [21,67].

7.1 Background on Integrated Inductors

7.1.1 Conventional Integrated Inductors

For integrated spiral inductors implemented using standard copper technology, a plethora of loss mechanisms impact their performance in mixed-signal systems [23, 56,64,65,68,233–240]. Figure 7.1 displays the electromagnetic effects in the inductor’s conductors and in the substrate below the inductor. The physical inductance is determined based on the current flowing in the conductors (self-inductance) and reinforced by the current flowing in the same direction in adjacent turns (mutual in-
ductance) of the spiral inductor [56,64]. Resistive losses in the inductor’s conductors are increased at high frequencies due to non-uniform current distribution resulting from skin and proximity effects [64,68,233–237]. Magnetically induced eddy currents produced in the substrate below the inductor affect the inductance and resistance of the inductor, especially on low resistivity substrates [23,56,65,238]. Furthermore, capacitive coupling between the conductors and substrate leakage currents decrease the energy stored in the inductor [233–235,240].

In addition to the square planar geometry depicted in Figure 7.1, integrated inductors can also be fabricated in octagonal and circular configurations in some man-
ufacturing processes. For a given set of geometric parameters, such as the number of turns in the inductor; the inductor's diameter; the width of the inductor's conductors; and the spacing between the inductor's conductors, the difference between the quality factors of circular, octagonal, and square spiral inductors implemented in copper technology is typically on the order of 10% with octagonal and circular inductors providing slightly better per unit area inductance [23,233,239].

Important figures of merit for spiral inductors in mixed-signal circuit applications include the quality factor and effective inductance. The quality factor is defined as

\[ Q = \frac{E_{\text{Stored}}}{E_{\text{Dissipated}}} = \frac{\text{Im}(Z)}{\text{Re}(Z)} \] (7.1)

where \( E_{\text{Stored}} \) is the energy stored in the inductor, \( E_{\text{Dissipated}} \) is the energy dissipated by the inductor parasitics, and \( Z \) is the input impedance of the inductor [23]. Note that \( Q \) depends on the operating frequency of the inductor. The effective inductance is defined as

\[ L_{\text{eff}} = \frac{\text{Im}(Z)}{\omega} \] (7.2)

where \( \omega \) is the operating frequency of the inductor in radians per second. Other important figures of merit include the self-resonant frequency of the inductor, where both \( Q \) and \( L_{\text{eff}} \) are 0, and the area consumed by the inductor. The resistance of the conductors significantly degrades the inductor's quality factor. Therefore, new technologies that can lower the overall resistance have the potential to substantially
improve the quality factors of integrated inductors, which could lead to large performance improvements in higher-level mixed-signal circuits.

### 7.1.2 Background on Nanotube-Based Inductors

While carbon nanotubes have been studied for on-chip interconnect applications, the modeling and design of on-chip inductors based on carbon nanotubes has not been extensively investigated for mixed-signal circuit applications in previously published research. Iron-filled nanotube inductors have been realized using carbon nanotube-polystyrene composite films with experimentally measured inductance values of 0.3 \( \mu H \) at 1 MHz [241]. However, the quality factors of the iron-filled nanotube-based inductors were not reported, and the electrical characteristics of the structures were only measured up to 1 MHz. Furthermore, the large size of the composite films (30 x 15 x 2 mm) poses a significant challenge for on-chip integration [241].

Coiled carbon nanotubes have also been suggested for inductors in sensing applications due to their solenoidal structure [242-244]. Given the relatively high measured resistivity of coiled carbon nanotubes (1.5 \( \Omega \cdot m \)) and the possibility that current may flow between adjacent turns in the solenoidal structure [245], coiled carbon nanotubes may not be able to provide sufficient quality factors for future mixed-signal circuit applications. Furthermore, manufacturing difficulties associated with controlling the length, diameter, and spacing between turns for coiled carbon nanotubes may significantly limit their potential for on-chip integration [242].
Nanotube inductors realized using an individual SWCNT have also been proposed [246], but as we demonstrate in Section 7.2.3, the quality factor of an inductor constructed using an individual nanotube is typically less than 1, which is not sufficient for RF circuit applications. Consequently, more complex nanotube-based structures must be leveraged for on-chip inductors. SWCNT bundles are an attractive solution for high quality integrated inductors due to the low resistance provided by the parallel conduction channels of the nanotubes in the bundle. Since carbon nanotube bundle-based inductors can leverage the extensive manufacturing technology being developed for the integration of nanotube bundle-based on-chip interconnect [3], we believe that carbon nanotube bundle-based inductors have a greater chance of being physically realized in the IC manufacturing process than previously proposed iron-filled nanotube inductors and inductors based on coiled carbon nanotubes. Therefore, in the remainder of this chapter, we focus on the modeling and design of nanotube bundle-based inductors.

7.2 Modeling and Design of CNT Based Inductors

To achieve high performance integrated inductors in future process technologies, we propose the utilization of SWCNT bundles as conductors in integrated spiral inductors as depicted in Figure 7.2. To determine the performance integrated inductors constructed using SWCNT bundle-based wires, we leverage the equivalent RLC model that we developed in Chapter 3. In the following sections, we develop modeling tech-
Carbon x Nanotube-Based Inductor

Figure 7.2: Nanotube-based inductor utilizing SWCNT bundle conductors.

...niques for current redistribution in SWCNT bundles, which can have an important impact on the quality factors of integrated inductors. We also discuss important design considerations for nanotube-based inductors.

7.2.1 Modeling Current Re-Distribution in SWCNT Bundles

For integrated spiral inductors implemented in standard copper interconnect, current redistribution due to skin and proximity effects can significantly increase the overall resistance [64, 233, 236, 237]. To accurately evaluate SWCNT bundles for integrated inductor applications, we must examine the current distribution in nanotube-based wires to determine if it has an analogue to skin and proximity effects in copper wires. Therefore, we have developed a model for current redistribution in SWCNT bundles that couples the resistance and inductance of the bundle. Expanding the inductance model for SWCNT bundles developed in Chapter 3, the magnetoquasistatic impedance of a bundle of SWCNT can be calculated using the following Partial Ele-
ment Equivalent Circuit (PEEC) formulation:

\[
Z_{\text{tot}} = \begin{bmatrix}
Z_1 & j\omega M_{m12} & \cdots & j\omega M_{m1n} \\
 j\omega M_{m21} & Z_2 & \cdots & j\omega M_{m2n} \\
 \vdots & \vdots & \ddots & \vdots \\
 j\omega M_{mn1} & j\omega M_{mn2} & \cdots & Z_n
\end{bmatrix}
\]  

(7.3)

\[
Z_i = j\omega (L_{mi} + L_{ki}) + R_{\text{toti}}
\]  

(7.4)

where \(L_{mi}\) is the partial self-inductance of the \(i\)th SWCNT in the bundle, and \(M_{mj}\) is the partial mutual inductance between the \(i\)th and \(j\)th SWCNTs for all \(n\) SWCNTs in the bundle. Similarly, \(L_{ki}\) and \(R_{\text{toti}}\) are the kinetic inductance and total resistance of the \(i\)th SWCNT in the bundle. The total frequency dependent resistance and loop inductance of an individual SWCNT bundle can be determined by solving

\[
v = Z_{\text{tot}}i
\]  

(7.5)

\[
v = [V_{\text{bias}}, V_{\text{bias}}, \ldots, V_{\text{bias}}]^T
\]  

(7.6)

\[
i = [I_1, I_2, \ldots, I_n]^T
\]  

(7.7)

for \(i\) where \(V_{\text{bias}}\) is the applied bias voltage, and \(I_i\) is the current flowing through the \(i\)th SWCNT in the bundle. Since SWCNT bundles with dimensions on the order of 1 \(\mu m\) will have approximately \(10^6\) individual nanotubes, applying the formulation in (7.5) directly to calculate the impact of current redistribution is intractable. Using
an approach similar to the *equivalent conductivity model* discussed in Chapter 3, we approximate the nanotube bundle as a current carrying conductor with a finite number of filaments, which closely matches the results obtained by modeling each nanotube discretely. In order to extend the formulation in (7.5) to nanotube-based integrated spiral inductors, we have modified the field solver, FastHenry [218], to include both the kinetic inductance and contact resistance of the SWCNT bundles.

Using the proposed modeling technique for current redistribution due to inductive effects in SWCNT bundles, we simulated the high frequency resistance of bundles with various $w_b$ values. The results are displayed in Figure 7.3. For bundles with the relatively small width value of 25 nm, the current does not re-distribute within the bundle until high frequencies since the resistance is large compared to the inductance. For bundles with $w_b$ values larger than 1 $\mu$m, the resistance can increase significantly due

![Figure 7.3:](image-url)
to current redistribution for frequencies below 10 GHz as depicted in Figure 7.3a. For a square bundle with a cross-sectional dimension of 3 μm, the resistance can become twice as large as its DC value. The impact of current redistribution on inductance is relatively small as displayed in Figure 7.3b. Furthermore, the impact of kinetic inductance is relatively small for frequencies below 10 GHz as depicted in Figure 7.3c. For an SWCNT bundle operating at 10 GHz with a width of 3 μm, the decrease in high frequency resistance due to kinetic inductance is only 2%. We observe similar results for current redistribution due to the proximity effect between two SWCNT bundles as displayed in Figure 7.3c. Since the resistance can increase by a factor of 2 over its DC value due to current redistribution in SWCNT bundles, inductive current redistribution in nanotube-based integrated inductors must be captured.

7.2.2 Impact of Inductor Geometry on Resistance

Given the relationship between the contact and ohmic resistance of SWCNT bundles, the inductor's geometry will play an important role in determining the behavior
of nanotube bundle-based inductors. Circular and octagonal spiral inductors could conceivably be constructed from a single nanotube bundle since the bending angle is relatively small as depicted in Figure 7.4. For bending angles of 45 degree or less, the resistive increases due to nanotube deformation are insignificant [247]. For circular and octagonal spiral inductors, the bundle length will be on the order of 1 mm for typical inductance values and geometries. Therefore, the ohmic resistance will essentially be the sole contributor to the overall resistance of the nanotube-based inductor.

Square spiral inductors will likely require a separate metal-nanotube bundle contact at each corner as depicted in Figure 7.4 since nanotubes bent at 90 degrees angles can experience significant resistive increases [247]. Therefore, the contact resistance will play a larger role in determining the overall resistance of the square SWCNT bundle-based inductor. However, the square nanotube-based inductor geometry will most likely be easier to fabricate than the circular geometry since the square geometry only requires the horizontal linear integration of nanotube bundles, which is also needed for the fabrication of standard nanotube-based interconnect. In contrast, the realization of the circular inductor geometry will necessitate the development of more sophisticated directional nanotube growth techniques to achieve the curved circular structure. Using several inductor design examples, we discuss the relative impact of the different sources of resistance on the predicted quality factor of nanotube bundle-based inductors in Section 7.3.1.
7.2.3 Impact of Kinetic Inductance on Inductor Design

Given the large theoretical value of kinetic inductance, it is reasonable to attempt to exploit it to achieve high density on-chip inductors. However, the quality factor of the realized on-chip inductors is equally important for mixed-signal applications. Without considering capacitive parasitics and resistive increases due to current redistribution in the conductors, an upper bound on the quality factor of an integrated inductor is given by the inductive reactance to resistance ratio \( \frac{\omega L}{R_{DC}} \), where \( R_{DC} \) is the resistance of the inductor's conductors at low frequencies.

To determine the maximum achievable quality factor when considering the kinetic inductance alone, we leverage the ratio of kinetic inductive reactance to resistance \( \frac{\omega L_{\text{kin}}}{R} \) results for various operating frequencies and \( d_t \) values from Figure 5.7b. For the kinetic inductance alone to have a relatively significant contribution to the overall quality factor of the inductor \( (Q \approx \frac{\omega L_{\text{kin}}}{R} \approx 1) \), the operating frequency must approach 100 GHz and \( d_t \) must be relatively large, which reduces the overall resistive advantages of SWCNT bundles. Therefore, for frequencies below the typical self-resonant frequency of integrated spiral inductors, leveraging the kinetic inductance alone will produce inductors with low quality factors. Consequently, as in the case of standard copper-based spiral inductors, the magnetic inductance must be leveraged to produce high quality nanotube inductors. Furthermore, since the magnetic inductance is several orders of magnitude smaller than the kinetic inductance for individual SWCNTs [165], inductors constructed using individual SWCNTs [246] will
also have quality factors less than 1. Therefore, nanotube bundles are necessary to provide the parallel conduction channels required to sufficiently lower the resistance to a level that provides acceptable quality factors for on-chip mixed-signal circuit applications.

7.2.4 Modeling SWCNT Bundle-Based Inductors

To model the quality factor, effective inductance, and self resonant frequency of SWCNT bundle-based integrated spiral inductors, we utilize the frequency-dependent eleven-element $\pi$-model developed in [64]. To determine the high frequency resistance and the physical inductance of the nanotube-based conductors, we utilize the PEEC-based described in Section 7.2.1. We utilize the distributed capacitance model from [240] to determine the effective capacitance between adjacent bundles in the inductor with a per unit length physical capacitance determined using the SWCNT bundle capacitance model described in Chapter 3. We assume that the substrate beneath the inductor is realized using standard silicon technology. To model the resistive and inductive impact of magnetically induced substrate eddy currents on the silicon substrate, we utilize the complex image theory-based formulation from [56]. We assume that the capacitive coupling between the SWCNT bundle-based inductor and the substrate is proportional to the area occupied by the inductor's conductors. Therefore, we model the parasitic capacitance between the SWCNT bundles in the
inductor and the substrate through the oxide layer using [234]

\[ C_{ox} = \frac{l_i w_b \varepsilon_{ox}}{2 h_g} \quad (7.8) \]

where \( l_i \) is the total length of the inductor's conductors, \( \varepsilon_{ox} \) is the permittivity of the inter-metal layer dielectric, and \( h_g \) is the distance between the bundles that compose the inductor and the substrate. Similarly, the capacitive losses in the silicon substrate are captured using [234]

\[ C_{si} = \frac{l_i w_b C_{sub}}{2} \quad (7.9) \]
\[ R_{si} = \frac{2}{l_i w_b G_{sub}} \quad (7.10) \]

where \( C_{sub} \) and \( G_{sub} \) are per unit length constants for the substrate capacitance and conductance, respectively. Leveraging the proposed model for SWCNT bundle-based inductors, we can predict their performance versus spiral inductors implemented in standard copper technology.

### 7.3 Results

#### 7.3.1 Evaluating the Performance of CNT-Based Inductors

To evaluate the performance improvement provided by nanotube-based inductors over those implemented using standard copper interconnect, we utilized the model
Figure 7.5: (a) Quality factor and (b) resistance for circular spiral inductors with SWCNT bundles and standard copper conductors. Note that the contact resistance has a minimal impact on the inductor's performance.

described in Section 7.2.4 to simulate a 4-turn spiral inductor with an 8 $\mu m$ conductor width, 2.0 $\mu m$ conductor thickness, 0.5 $\mu m$ spacing between conductors, and a 200 $\mu m$ inductor diameter. We simulate both circular and square inductor geometries to highlight the difference in overall resistance and quality factor caused by the SWCNT contact resistance. We assume that the conductors are fabricated 6 $\mu m$ over a high resistivity substrate for both the copper and SWCNT bundle-based inductors. For
Figure 7.6: (a) Quality factor and (b) resistance for square spiral inductors with SWCNT bundles and standard copper conductors. Note that the contact resistance has a significant impact on the inductor's performance.

the SWCNT bundles, we assume that the nominal contact resistance is 20 kΩ per nanotube.

Figure 7.5 displays the quality factors and resistances for circular spiral inductors implemented with SWCNT bundles and standard copper conductors. Note that the contact resistance has only a small impact on the inductor’s performance since the circular geometry allows for the utilization of a single nanotube bundle to implement
the entire inductor. The quality factor that can be obtained for nanotube-based inductors greatly depends on the achievable $P_m$ value. When $P_m = 1/3$, the quality factor of the inductor is only increased by 8% over the quality factor of the standard copper inductor with the same geometry. However, when $P_m$ is increased to 2/3 and 1, the quality factor of the circular integrated inductor increases by 80% and 144%, respectively, primarily due to the decreased resistance provided by the SWCNT bundle-based inductors as depicted in Figure 7.5b. Note that based on the resistance results presented in Figure 5.10, the quality factors of inductors implemented utilizing large-diameter MWCNT bundles will be approximately the same as the quality factors obtained for SWCNT bundles with $P_m = 2/3$. The predicted quality factor of the nanotube-based inductor is 29.2 when $P_m = 1$, which will provide significantly lower loss for spiral inductors in fully integrated mixed-signal circuits.

Figure 7.6 displays the quality factors and resistances for square spiral inductors implemented with SWCNT bundles and standard copper conductors. Note that the contact resistance has a significantly larger impact on the square inductor's performance than it does for the circular inductor since metal contacts are required at each corner of the inductor. The contact resistance of SWCNT bundle-based square inductors decreases the quality factor by 13%, 11%, and 10% for bundles with $P_m$ values for 1/3, 2/3, and 1, respectively. For the square geometry, the SWCNT bundle-based square inductor with $P_m = 1/3$ has a slightly lower quality factor than its copper counterpart, while when $P_m = 1$, the quality factor is increased by 126%.
Figure 7.7: Quality factor for circular spiral inductors with SWCNT bundles and standard copper conductors implemented on low and high resistivity silicon substrates and implemented in silicon-on-insulator technology.

7.3.2 Impact of Substrate Parasitics

Figure 7.7 displays the quality factors for circular spiral inductors with the aforementioned geometric parameters with SWCNT bundles and standard copper conductors implemented on low and high resistivity silicon substrates and in silicon-on-insulator (SOI) technology. At low frequencies (<1.5 GHz), the quality factors of the inductors are primarily determined by the resistance of the conductors. As the oper-
ating frequency of the inductors increases, capacitive coupling and leakage currents to the substrate also begin to degrade their quality factors. For inductors fabricated over substrates with low resistivity, magnetically induced substrate eddy currents also decrease the effective inductance and increase the effective resistance.

For the inductors implemented above low and high resistivity silicon substrates, the maximum quality factors occur at approximately 2 and 3.5 GHz, respectively, as depicted in Figure 7.7. The maximum quality factor occurs at approximately 12 GHz for the inductors implemented in SOI technology due to the lower substrate losses. The percentage increase for the maximum quality factor is 118%, 144% and 181% for SWCNT bundle-based inductors \((P_m = 1)\) implemented on low and high resistivity silicon substrates and implemented in SOI technology, respectively, compared to copper-based integrated inductors. Therefore, the lower resistances of the SWCNT bundle-based inductors provide a significant quality factor improvement over copper-based inductors in a large frequency range regardless of magnitude of the losses caused by substrate losses. Note that the quality factors obtained by the model for the copper-based conductors are on the same order as those measured for inductors fabricated on silicon substrates [233, 234] and in SOI technology [248].

### 7.3.3 General Performance Improvement

To obtain a more general prediction of the expected performance improvement provided by nanotube-based inductors, we simulated approximately 50,000 induc-
Figure 7.8: Distribution of the percentage increases in the quality factor of circular and square nanotube-based inductors over those implemented with standard copper conductors for different $P_m$ values. Approximately 50,000 cases were simulated.

tor geometry and operating frequency combinations for both SWCNT bundles and copper conductors and for both circular and square geometries. Figure 7.8 displays the distribution of the percentage increases in the quality factor of nanotube-based inductors with $P_m$ values ranging from 1/3 to 1 over those implemented with standard copper interconnect. For circular nanotube inductors, the average percentage increases in quality factor are 15%, 109%, and 214% for $P_m$ values of 1/3, 2/3, and 1, respectively. The largest percentage increase in quality factor obtained was 324% for a circular inductor geometry with $P_m = 1$. For square nanotube inductors, the average percentage increases in quality factor are -1%, 83%, and 174% for $P_m$ values of 1/3, 2/3, and 1, respectively. The largest percentage increase in quality factor obtained for a square inductor geometry was 305%. The average decreases in quality factor due to
the additional metallic contacts required for square inductor geometries are 16%, 26%, and 40% for $P_m$ values of 1/3, 2/3, and 1, respectively. Therefore, nanotube-based integrated inductors have the potential to provide significant performance improvement over standard copper inductors, especially for circular geometries, if the $P_m$ value can be increased beyond its nominal value of 1/3.

7.3.4 Impact on Analog Circuit Performance

To demonstrate the performance implications of nanotube-based inductors on higher-level analog circuits, we optimized narrow-band LNA designs operating at 2.4 GHz using both nanotube bundle and copper-based circular and square spiral inductors. LNAs are critical circuits for the performance of integrated wireless applications since they amplify the weak received signal from the antenna while generating minimal noise [67]. We utilize the inductively degenerated cascode LNA topology from [67] and generate optimal LNA circuits in terms of noise figure using the automated design methodology from [21] with optimal inductors designed using [22, 63, 66]. We enforce a power dissipation constraint of 10 mW, a gain constraint of 10 dB, and constraints on $S_{11}$ and $S_{22}$ of -10 dB during the LNA optimization process.

Figure 7.9 displays the noise figure of optimized narrow-band LNAs operating at 2.4 GHz implemented with circular and square nanotube-based and standard copper inductors. The design that employs circular standard copper inductors has a minimum noise figure of 0.76 dB at 2.4 GHz, while the optimized LNA designs that employ
circular nanotube-based inductors have minimum noise figures of 0.73 dB, 0.59 dB, and 0.51 dB at 2.4 GHz for $P_m$ values of 1/3, 2/3, and 1, respectively. Similarly, for the LNA designs that employ square inductors, the minimum noise figure is 0.89 dB at 2.4 GHz in the copper inductor case, and the minimum noise figures are 0.85 dB, 0.68 dB, and 0.60 dB at 2.4 GHz in nanotube-based inductors with $P_m$ values of 1/3, 2/3, and 1, respectively. Therefore, when $P_m = 1$ for nanotube-based inductors, the noise figure of the optimized LNA decreases by 33% compared to an optimized LNA implemented using copper-based inductors in both the circular and square cases. In addition to decreasing the noise generated by the inductors themselves, the decreased resistance of the nanotube-based inductors allows the LNA optimization routine to utilize a larger range of inductance values for impedance matching, which allows for more optimal transistor width values in the amplifier for noise minimization [21].
Figure 7.10: Trade-off between power consumption and optimal noise figure for optimized narrow-band LNAs operating at 2.4 GHz implemented with nanotube-based inductors and standard copper inductors.

The lower noise provided by the higher quality factors achieved by the nanotube-based inductors can be leveraged to decrease the power consumption of integrated LNAs. Figure 7.10 displays the trade-off between power consumption and optimal noise figure for optimized narrow-band LNAs operating at 2.4 GHz implemented with circular nanotube-based and standard copper inductors. LNAs implemented with circular nanotube-based inductors with $P_m$ values of 1/3, 2/3, and 1 require 17%, 68%, and 80% less power, respectively, to achieve the noise figure of an LNA implemented with standard copper inductors. Note that optimized LNAs with square nanotube-based inductors achieve similar percentage reductions in power consumption compared to LNAs with square copper inductors. Therefore, LNAs implemented with nanotube-based inductors can achieve a particular noise requirement with significantly less power consumption than LNAs implemented with copper inductors.
Chapter 8

Carbon Nanotube-Based

Integrated Capacitors

In current VLSI applications, integrated capacitors play an important role in determining performance, reliability, and on-chip area utilization. Numerous analog and wireless circuits such as low noise amplifiers (LNA) [21,22,56–77], voltage controlled oscillators [17], and RF filters [19,20,78] depend on high density integrated capacitors with low loss. Furthermore, integrated decoupling capacitors are utilized to reduce the voltage variation from the external power supply in digital and mixed-signal systems [18]. The major limitation of current metal-insulator-metal (MIM) and metal-oxide-semiconductor (MOS) capacitor technologies is the relatively small capacitance per area, which impacts the chip area consumed by mixed-signal systems and limits the maximum capacitance value that can be realized on-chip [1]. The qual-
ity factor of MIM and MOS capacitors can also limit circuit performance [24,25]. To improve the density and quality factor of integrated capacitors for future mixed-signal systems, alternative technologies must be investigated.

Carbon nanotubes are a promising technology for future high density on-chip capacitors due to their low resistivity and nanoscale dimensions. Both SWCNT and MWCNT based capacitors have been physically realized for sensing and memory applications [155,249]. Most of the previous theoretical studies have primarily focused on quantifying the physical capacitance of SWCNTs and MWCNTs [206,250]. However, modeling the impact of the resistive and inductive parasitics on the capacitor's performance is crucial for mixed-signal applications. While SWCNT bundle-based capacitors have been modeled considering parasitic effects [174], the performance of capacitors based on MWCNTs has yet to be explored.

In this chapter, we investigate three possible high density integrated capacitor configurations based on MWCNTs. We develop an RLC model for the MWCNT-based capacitor configurations and examine the design trade-off between capacitance per area and losses due to parasitic resistance and inductance. The results indicate that the proposed MWCNT-based capacitor configurations can potentially offer orders of magnitude larger capacitance per area and greater quality factors compared to traditional metal-based integrated capacitors, which could enable more compact mixed-signal systems with greater performance. This chapter highlights the performance and capacitive density limits of potential MWCNT-based capacitor structures.
8.1 MWCNT-Based Capacitors

To leverage MWCNTs for capacitor applications, several different configurations are possible. An individual MWCNT can be utilized to form a coaxial capacitor where the inner shells of the MWCNT form one terminal and the outer shells of the MWCNT are utilized as the other terminal as depicted in Figure 8.1a. This configuration can be physically realized by laterally displacing the inner and outer shells of the MWCNT as depicted in Figure 8.1b [100]. The capacitance value and the losses associated with the inter-shell tunneling resistance ($R_{tuni}$) are related to the number of unconnected shells ($N_{shells}$) between the connected inner and outer shells of the MWCNT. To achieve larger capacitance values and less sensitivity to MWCNT
We envision three possible parallel MWCNT-based capacitor configurations. Multiple individual MWCNT capacitors (IMC) can be connected together in parallel as depicted in Figure 8.2a. In this configuration, large per unit area capacitance values can be achieved between the inner and outer shells of each MWCNT. Another possible MWCNT-based capacitor configuration is the MWCNT bundle capacitor (MBC) depicted in Figure 8.2b where all of the shells in a given MWCNT are connected to either the cathode or the anode of the capacitor. The cathode and anode MWCNTs are interleaved to form a high density interdigitated MWCNT bundle-based capacitor. In this configuration, the major loss mechanisms include the resistance of the MWCNTs and the inter-tube coupling between adjacent MWCNTs ($R_{int}$). The third proposed MWCNT-based capacitor configuration, depicted in Figure 8.2c, combines the previously discussed individual and bundled MWCNT configurations into
a hybrid MWCNT bundle capacitor (HMBC). This configuration leverages both the capacitance between shells in a given MWCNT and the capacitance between adjacent MWCNTs. By leveraging both possible sources of capacitive coupling, a larger per unit area capacitance is possible.

As we discuss in Section 8.3, MWCNTs with relatively short length values \( (L) \) provide the largest quality factors. Therefore, MWCNT-based capacitors could be vertically integrated (Figure 8.1c) and fabricated using similar techniques to those that will potentially be employed to realize MWCNT-based vias in future interconnect applications [2, 3, 27, 28, 157, 158, 163]. The MBC configuration will be significantly easier to implement than the IMC or HMBC configurations since the MBC configuration does not require separate physical connections to the inner and outer shells of each MWCNT. The IMC and HMBC configurations can be physically realized by laterally displacing the inner and outer shells of the MWCNT as depicted in Figure 8.1b [100]. This has been experimentally accomplished by applying electrostatic forces to displace the inner shells of individual MWCNTs [251, 252]. However, applying this technique to MWCNT bundles will require additional experimental research. Consequently, from a fabrication standpoint, the MBC configuration is the most promising of the three proposed MWCNT-based capacitor configurations.
8.2 Modeling of MWCNT Capacitors

8.2.1 Circuit Model for MWCNT-Based Capacitors

To predict the performance of the three proposed MWCNT-based capacitor configurations, we have developed an RLC model that captures the resistive and inductive parasitics that impact the quality factor ($Q$) of the capacitor. For the IMC configuration, the equivalent circuit model consists of only the *inner MWCNT shells* and the *outer MWCNT shells* portions of the circuit model displayed in Figure 8.3. To model the MBC configuration, the equivalent circuit model contains only the *inner MWCNT shells* and the *external MWCNTs* portions of the circuit model. Note that in this configuration the inner MWCNT shells portion of the circuit model captures the electrical characteristics of all of the shells in a given MWCNT. The entire RLC circuit model is utilized to characterize MWCNT-based capacitors in the HMBC configuration.
8.2.2 Calculation of Circuit Model Elements

In the equivalent circuit model depicted in Figure 8.3, $R_{i1}$ represents the total resistance of the inner shells of an MWCNT capacitor, which includes contributions from the per unit length ohmic resistance ($R_o$) due to phonon scattering and from the lumped intrinsic ($R_i$) and contact resistances ($R_c$) of each MWCNT shell, which are calculated using the model we developed in Chapter 3. The total resistance of the inner shells is the parallel combination of the total resistance of each shell,

$$R_{i1} = \frac{2/3}{\sum_{j=1}^{N_{inner}} \left( \frac{1}{R_{oj} + R_{ij} + R_{oj}} \right)},$$

where $N_{inner}$ is the number of conducting shells that comprise the inner electrode of the MWCNT-based capacitor; and $R_{oj}$, $R_{ij}$, and $R_{oij}$ are the ohmic, intrinsic, and contact resistances of the $j$th shell. For the MBC configuration, $N_{inner}$ equals the total number of total shells ($N_s$) in the MWCNT.

$R_{i2}$ is the total resistance of the outer shells of an MWCNT capacitor. For the IMC and HMBC configurations, $R_{i2}$ is the parallel combination of the total outer shell resistances and is calculated in a similar manner to (8.1). Similarly, $R_e$ is the total resistance of the external MWCNTs in the MWCNT bundle capacitor. In the MBC configuration, $R_e$ is the parallel combination of the resistances of all of the shells in the MWCNT, while in the HMBC configuration, $R_e$ is just the parallel combination of the outer shell resistances. Note that the factor of $2/3$ is included in the calculation.
of $R_{i1}$, $R_{i2}$, and $R_e$ as shown in (8.1) to accurately capture the effective distributed resistance of the interdigitated electrodes [24].

In terms of inductance, the magnetic inductance will be relatively insignificant compared to the kinetic inductance since MWCNT-based capacitors with relatively short $L$ values provide the largest quality factors. Consequently, the total inductance of the inner shells ($L_{i1}$), the outer shells ($L_{i2}$), and the external shells ($L_e$) for the three MWCNT-based capacitor configurations presented in Figure 8.2 is the parallel combination of the kinetic inductances for each conducting shell calculated using the model we developed in Chapter 3 multiplied by a factor of 2/3 to capture the effective distributed inductance.

The total capacitance of an MWCNT-based capacitor is determined by the series combination of its total effective electrostatic and quantum capacitances. The total quantum capacitance of the inner shells ($C_{q11}$), the outer shells ($C_{q12}$), and the external shells ($C_{qe}$) is the parallel combination of the quantum capacitances for each conducting shell calculated using the model we developed in Chapter 3 and multiplied by a factor of 2/3 to capture the effective distributed quantum capacitance. The electrostatic capacitance between the inner and outer conducting shells of an individual MWCNT is

$$C_{ci} = \frac{2\pi \varepsilon L}{\ln \left( \frac{d_{outer}}{d_{inner}} \right)}$$

(8.2)

where $d_{outer}$ is the diameter of the innermost shell in the outer conducting shells and $d_{inner}$ is the diameter of the outermost shell in the inner conducting shells [206].
Table 8.1: Numerical values for parameters in the model for $C_{ce}$.

For the IMC and HMBC configurations, we assume that each MWCNT in the bundle has 3 adjacent MWCNTs of opposite polarity, which provide an additional external coupling capacitance ($C_{ce}$) that depends on the outer diameter ($d_{out}$) and edge-to-edge spacing ($S_t$) between the MWCNTs in the bundle. Since no standard closed-form model exists for the capacitance of this 4 conductor configuration, we have developed a parameterized analytical model based on extensive field solver simulations using COMSOL Multiphysics to calculate $C_{ce}$,

$$C_{ce} = \left( \frac{L_e}{\beta_{11} \varepsilon_0} \right) 10^{C_{log}}, \quad (8.3)$$

where $C_{log}$ is a ninth-order polynomial function,

$$C_{log} = \beta_1 r^9 + \beta_2 r^8 + \cdots + \beta_8 r^2 + \beta_9 r + \beta_{10}, \quad (8.4)$$

which depends the logarithm of the ratio between $d_{out}$ and $S_t$, $r = \log_{10}(d_{out}/S_t)$. The numerical values for $\beta_1 \cdots \beta_{11}$ used to calculate $C_{ce}$ are determined using multivariate linear least squares regression and are listed in Table 8.1. The model is valid for $0.01 \leq d_{out}/S_t \leq 1000$. From an extensive set of field solver simulations using COMSOL
Multiphysics, we find that the average and maximum errors of the analytical model for $C_{oe}$ are 0.3% and 0.6%, respectively.

Both the inter-shell resistance ($R_{tuni}$) between the shells within an individual MWCNT and the inter-tube resistance ($R_{tc}$) between adjacent MWCNTs greatly impact the achievable quality factor for MWCNT-based capacitors. We calculate the inter-shell tunneling resistance between adjacent shells in the MWCNT-based capacitor using the model we developed in Chapter 3. Since approximately 1/3 of the possible nanotube chiralities are metallic, we assume that the average tunneling resistance between adjacent MWCNT shells is

$$R_{tuna} = \frac{R_{tunn} + 2R_{tuns}}{3}$$  \hspace{1cm} (8.5)

where $R_{tuns}$ and $R_{tuns}$ are the inter-shell tunneling resistance for metallic and semiconducting nanotubes, respectively. The total inter-shell resistance ($R_{tuni}$) is the summation of the inter-shell resistances for each pair of adjacent shells between the inner and outer conducting electrodes based on (8.5). We calculate the inter-tube resistance ($R_{tc}$) between two MWCNTs based on the model we developed in Chapter 3. Leveraging the developed RLC circuit model, we are able to efficiently characterize and design MWCNT-based capacitors with high densities and quality factors.
Table 8.2: MWCNT-based capacitors with the highest capacitance per unit area for quality factors of 50, 100 and 250.

<table>
<thead>
<tr>
<th>Cap. Config.</th>
<th>Quality Factor</th>
<th>Cap. (pF/μm²)</th>
<th>dₜ (nm)</th>
<th>N_ shells</th>
<th>L (μm)</th>
<th>Sₜ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IMC 50</td>
<td>50</td>
<td>6.50</td>
<td>5.7</td>
<td>0</td>
<td>1.93</td>
<td>0.34</td>
</tr>
<tr>
<td>IMC 100</td>
<td>100</td>
<td>3.62</td>
<td>5.7</td>
<td>0</td>
<td>1.06</td>
<td>0.34</td>
</tr>
<tr>
<td>IMC 250</td>
<td>250</td>
<td>1.19</td>
<td>5.0</td>
<td>1</td>
<td>0.50</td>
<td>0.34</td>
</tr>
<tr>
<td>MBC 50</td>
<td>50</td>
<td>6.01</td>
<td>5.7</td>
<td>N/A</td>
<td>2.41</td>
<td>0.89</td>
</tr>
<tr>
<td>MBC 100</td>
<td>100</td>
<td>3.50</td>
<td>5.7</td>
<td>N/A</td>
<td>1.54</td>
<td>1.17</td>
</tr>
<tr>
<td>MBC 250</td>
<td>250</td>
<td>1.67</td>
<td>5.7</td>
<td>N/A</td>
<td>0.73</td>
<td>1.26</td>
</tr>
<tr>
<td>HMBC 50</td>
<td>50</td>
<td>5.18</td>
<td>5.0</td>
<td>0</td>
<td>1.66</td>
<td>1.26</td>
</tr>
<tr>
<td>HMBC 100</td>
<td>100</td>
<td>5.30</td>
<td>5.7</td>
<td>0</td>
<td>0.96</td>
<td>0.80</td>
</tr>
<tr>
<td>HMBC 250</td>
<td>250</td>
<td>2.23</td>
<td>5.7</td>
<td>0</td>
<td>0.5</td>
<td>6.00</td>
</tr>
</tbody>
</table>

8.3 Performance of MWCNT Capacitors

To design MWCNT-based capacitors, dₜ, N_ shells, L, and Sₜ are important degrees of freedom that can be utilized to trade-off the capacitance per unit area and Q. We simulate each combination of these four parameters to determine their impact on the capacitor's quality factor and density at 1 GHz. We assume that the MWCNT inner-to-outer diameter ratio is 0.50 [106] and the contact resistance per conducting channel in the MWCNT is 12.5 kΩ. The quality factor for an MWCNT-based capacitor is $Q = \text{Im}(Z)/\text{Re}(Z)$ where $Z$ is the input impedance given by the RLC circuit model displayed in Figure 8.3.

By searching the dₜ, N_ shells, L, and Sₜ design space, we can locate MWCNT-based capacitor designs that maximize the trade-off between Q and the per unit area capacitance. Table 8.2 lists the geometric parameters for MWCNT-based capacitors optimized for $Q = 50$, $Q = 100$, and $Q = 250$. Note that the optimal MWCNT-based capacitor geometries typically have short L values, which reduce the impact of $R_{tuni}$ and $R_{te}$. Therefore, the quality factor for the MWCNT-based capacitor
Figure 8.4: Maximum achievable quality factors for a given capacitance per unit area for the three proposed MWCNT-based capacitor configurations.

increases for smaller \( L \) values since \( R_{\text{tun}} \) is minimized. Increases in \( N_{\text{shells}} \) lead to larger quality factors due to decreases in \( R_{\text{tun}} \), but larger \( N_{\text{shells}} \) values also increase the distance between the cathode and anode MWCNT shells, which reduces the per unit area capacitance. MWCNT-based capacitors with larger \( d_{\text{out}} \) values also increase \( Q \) since the inner and outer terminals have a greater number of conducting shells, which reduces both the series resistance and inductance. However, increasing \( d_{\text{out}} \) also reduces the per unit area capacitance.

Expanding the results provided by Table 8.2, Figure 8.4 displays the maximum achievable quality factors for a given capacitance per unit area for the three proposed MWCNT-based capacitor configurations, which establish the performance limits for the MWCNT-based capacitor configurations considered in this study. For densities
greater than $2 \ pF/\mu m^2$, the IMC and MBC configurations have approximately the same maximum achievable quality factors while the HMBC configuration achieves significantly larger maximum quality factors by leveraging both the internal ($C_d$) and external ($C_{ce}$) electrostatic capacitances. For capacitive densities less than $2 \ pF/\mu m^2$, the MBC configuration provides the largest quality factors since $R_{te}$ typically has a smaller impact on the quality factor than $R_{runi}$, which limits the maximum quality factor that can be achieved using the IMC and HMBC configurations. Given the fabrication challenges associated with the IMC and HMBC configurations as well as the higher achievable quality factors for the MBC configuration for capacitive densities less than $2 \ pF/\mu m^2$, the MBC configuration provides the most attractive balance between capacitive density, quality factor, and ease of fabrication for the three MWCNT-based capacitor structures considered in this study.

Since potential future IC-compatible fabrication techniques for MWCNT bundles may not be able to achieve the minimum theoretically possible spacing between nanotubes ($S_t = 0.34 \ nm$) as we discuss in Section 2.3, we also evaluate the maximum achievable quality factors for a given capacitance per unit area for the MBC MWCNT-based capacitor configuration with minimum allowed $S_t$ values ranging from 0.34 to 40.0 nm. The results are depicted in Figure 8.5. The capacitive density decreases by one to two orders of magnitude as the minimum allowed $S_t$ value increases from 0.34 to 40.0 nm. For larger $S_t$ values, the inter-tube resistance, $R_{te}$, will become extremely large, and therefore, it will have a negligible impact on the quality factor.
Figure 8.5: Maximum achievable quality factors for a given capacitance per unit area for the MBC MWCNT-based capacitor configuration with minimum allowed $S_t$ values of 40.0, 30.0, 25.0, 20.0, 15.0, 10.0, 5.0, 2.0, and 0.34 nm.

This causes the slope of the capacitive density versus quality factor lines in Figure 8.5 to increase, which indicates that it becomes easier to attain larger quality factors for geometries below a certain capacitive density threshold when the minimum allowed $S_t$ value is relatively large. Therefore, the larger $S_t$ values primarily impact the maximum possible capacitive density as opposed to the maximum possible quality factor.

Table 8.3 compares the optimized MWCNT-based capacitors ($Q = 100$) with SWCNT bundle-based capacitors [174], predicted MOS capacitors in the 2016 node of ITRS [1,25], and predicted MIM capacitors in the 2016 node of ITRS [1]. MWCNT-based capacitors achieve either greater or comparable quality factors to the alternative technologies with up to 3 orders of magnitude increase in capacitance per unit area.
Table 8.3: Comparison between future capacitor technologies.

<table>
<thead>
<tr>
<th>Capacitor Type</th>
<th>Capacitance (pF/μm²)</th>
<th>Quality Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Individual MWCNT Capacitor (IMC) - Minimum S₁ Value = 0.34 nm</td>
<td>3.62</td>
<td>100</td>
</tr>
<tr>
<td>MWCNT Bundle Capacitor (MBC) - Minimum S₁ Value = 0.34 nm</td>
<td>3.50</td>
<td>100</td>
</tr>
<tr>
<td>MWCNT Bundle Capacitor (MBC) - Minimum S₁ Value = 5.0 nm</td>
<td>1.05</td>
<td>100</td>
</tr>
<tr>
<td>MWCNT Bundle Capacitor (MBC) - Minimum S₁ Value = 40.0 nm</td>
<td>0.086</td>
<td>100</td>
</tr>
<tr>
<td>Hybrid MWCNT Bundle Capacitor (HMBC) - Minimum S₁ Value = 0.34 nm</td>
<td>5.30</td>
<td>100</td>
</tr>
<tr>
<td>Bundled SWCNTs - Minimum S₁ Value = 2.0 nm [174]</td>
<td>2.71</td>
<td>~100</td>
</tr>
<tr>
<td>Bundled SWCNTs - Minimum S₁ Value = 4.0 nm [174]</td>
<td>1.16</td>
<td>~100</td>
</tr>
<tr>
<td>MOS Capacitor (ITRS) 2016 node [1,25]</td>
<td>0.011</td>
<td>20 to 50</td>
</tr>
<tr>
<td>MIM Capacitor (ITRS) 2016 node [1]</td>
<td>0.010</td>
<td>&gt;50</td>
</tr>
</tbody>
</table>

over MOS and MIM capacitors. Even if the minimum allowed S₁ value is increased to 40.0 nm, which is 8x larger than what was experimentally realized using the CVD-based process in [3], MWCNT-based capacitors in the MBC configuration achieve one order of magnitude improvement in capacitance per unit area over MOS and MIM capacitors. The MWCNT-based capacitors achieve a similar capacitance per unit area to SWCNT bundle-based capacitors, and therefore, the availability and cost of potential future IC-compatible fabrication techniques for nanotube bundles will likely determine which type of nanotube will ultimately be utilized to realize high density capacitors in future mixed-signal VLSI applications.
Chapter 9

Conclusions and Future Research Directions

9.1 Conclusions

In this thesis, we develop modeling and design techniques for interconnect based on SWCNTs and MWCNTs, which we leverage to investigate the performance and reliability of nanotube-based interconnect solutions for on-chip communication and passive components in future mixed-signal VLSI applications. We create an equivalent RLC circuit model for individual and bundled SWCNTs and MWCNTs, which we utilize to investigate the performance and reliability of nanotube-based interconnect solutions. We develop design techniques for CNT-based interconnect structures to optimize their performance for on-chip communication. Using the developed equivalent circuit model for SWCNT and MWCNT bundles, we also examine the design
and potential performance advantages of nanotube-based inductors and capacitors for future mixed-signal VLSI applications.

The results indicate that nanotube-based interconnect solutions can provide a significant delay reduction over scaled copper wires for on-chip communication, and the performance advantages of CNT-based interconnect become more pronounced as process technology scales downward and the cross-sectional area of the wires decreases. Nanotube bundles with geometries optimized using the proposed design techniques can provide a significant delay reduction over non-optimized multi-walled and single-walled CNT bundles. In terms of reliability, we find that nanotube bundle interconnects are more susceptible to process variations than copper interconnects due to the additional statistical uncertainty caused by intra-bundle and inter-bundle variations in individual nanotube properties. Therefore, to realize nanotube-based interconnect with suitable reliability, significant control over sources of process variation will be required. Finally, the results indicate that CNT-based inductors and capacitors can provide significant increases in quality factor and density over passive components implemented in current semiconductor-based VLSI process technologies. If the manufacturing challenges associated with high density, IC-compatible parallel growth of CNT bundles can be overcome, the results presented in this study indicate that nanotube-based interconnect could successfully alleviate the on-chip communication and passive component performance bottlenecks that currently plague nano-scale integrated circuits for mixed-signal VLSI applications.
9.2 Future Research Directions

Based on the promising results for nanotube-based interconnect for mixed-signal VLSI applications presented in this study, several future theoretical and experimental research directions could continue to facilitate the development of CNT-based interconnect solutions. Since larger interconnect and device densities have significantly increased the impact of thermal effects and power consumption for nanoscale integrated circuits [1, 253–257], future modeling and design research for CNT-based interconnect solutions should capture the complex interaction between thermal and electrical properties and evaluate the performance and reliability implications of thermal effects versus standard copper interconnect. Initial research efforts are already underway in this area [258, 259]. Furthermore, given the complexity of current and future VLSI designs, high-level computer aided design tools must also be developed to fully leverage the potential performance advantages of nanotube interconnect in future mixed-signal VLSI systems [189]. These high-level CAD solutions will facilitate the system-level design of CNT-based interconnect on realistic VLSI systems [179, 180].

In terms of experimental research, additional investigation is still needed to fully empirically determine the electrical properties associated with bundled SWCNT and MWCNTs, particularly the measurement of magnetic inductive effects and the measurement of capacitive and inductive coupling to nearby metallic structures. While the relationship between resistance and thermal effects for individual SWCNTs and MWCNTs has been examined [260–272], extensive experimental investigations on
bundles of SWCNTs and MWCNTs pertaining to temperature dependent resistance and self-heating as well as the thermal-electrical impact of AC current are also needed to provide important empirical insights into the performance and reliability of future CNT-based interconnect solutions. The IC-compatible parallel growth of vertical and horizontal CNT bundles with sufficient CNT density for interconnect applications remains an important challenge that must be addressed. Overall, the modeling, design, and performance/reliability analysis of nanotube-based interconnect solutions and passive components presented in this study will help to guide these future theoretical and experimental research efforts toward the realization of this promising technology in future high performance nanoscale integrated circuits.
Bibliography


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