Reducing dynamic power consumption in next generation DS-CDMA mobile communication receivers

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Abstract

Reduction of the power consumption in portable wireless receivers is an important consideration for next-generation cellular systems specified by standards such as the UMTS, IMT2000. This paper explores the architectural design-space and methodologies for reducing the dynamic power dissipation in the Direct Sequence Code Division Multiple Access (DS-CDMA) downlink RAKE receiver. Starting with a reference implementation of the DS-CDMA RAKE receiver, we demonstrate design methodologies for achieving significant power reduction, while highlighting the corresponding performance trade-offs. At the algorithm level, we investigate the tradeoffs of reduced precision and arithmetic complexity on the receiver performance. We then present two architectures for implementing the reference and reduced complexity receivers, and analyze these architectures with respect to their dynamic power dissipation. Our findings report that reduction in precision from a 16 bit to a 10 bit data-path is found to yield significant power savings of 25.6% in the reference RAKE receiver architecture, with a performance loss of less than 1 dB. Further, a power reduction of upto 24.65% is achieved in a 16 bit data-path for the reduced complexity RAKE receiver compared to the reference architecture, with a performance loss of less than 2 dB. Although there is a tradeoff in performance, adaptive power saving is very important for mobile wireless terminals. The combined effect of reduced precision and complexity reduction leads to a 37.44% savings in baseband processing power.

1 Introduction

Achieving power-efficient architectures will be a major goal in the design of next-generation mobile communication receivers such as laptops, cell phones, PDA etc. Future portable receivers will need the ability to handle various multimedia data traffic irrespective of mobility, provide guaranteed Quality-of-service (QoS) requirements, and integrate multiple functionality (GPS, World Wide Web, e-commerce, etc.) simultaneously. The high bandwidth required by these applications implies that this functionality would come at the expense of a heavy drain on the available battery power. For example, the IMT Standard [8] for a mobile terminal specifies a target data-rate of 384 Kbps at bit error rates of the order of 10^{-3} to 10^{-7} in an urban outdoor terrain. Achieving these high levels of expected performance, as well as the required data-rates will call for the implementation of advanced algorithms in the design of such receivers. With rapidly improving integrated-circuit

(IC) technology as well as the decreasing cost of silicon area, there have been great advances in the ability to integrate the entire receiver chain on a single-chip (System-on-chip design). The point that has not been addressed in these designs is the system integration, with power minimization as a key constraint. This work explores the techniques and trade-offs involved in the design of power-efficient architectures for next-generation DS-CDMA mobile communication receivers.

Figure 1 shows the high-level description of the front-end in a wireless communication receiver. The architectures implemented in this paper are represented by the solid line blocks, while the dashed-line blocks are assumed to input the sampled wide-band signal and the estimated multi-path delays into the receiver. Further details regarding the implementation of the individual blocks can be found in [3]. The RAKE receiver unit forms an important constituent of a DS-CDMA mobile

Figure 1. Front-end description of a wireless communication DS-CDMA receiver.

receiver for performing single-user detection. The RAKE algorithm is a conceptually simple algorithm, however, its computational complexity increases linearly with the number of multi-path components being processed. Even though there has been considerable research investigating techniques for improving the performance of DS-CDMA RAKE receivers in fading multi-path channels, there has been comparatively little research on investigating methodologies for minimizing the power dissipation of the receiver architectures. A strength reduction technique has been described in [1] for reducing the on line power dissipation in the complex RAKE multipliers by up to 25%. Power reduction techniques for a spread spectrum based correlator have been described in [5] using a modified adder-tree structure and employing bus-invert coding. Low-power correlator architectures have been described in [11] that employ a partial correlation approach for reducing on-line power dissipation during code acquisition in WCDMA based systems. To the best of our knowledge, there has been very little work on developing a framework which analyzes the performance vs. power dissipation trade-offs in the context of mobile DS-CDMA RAKE receivers.

1.1 Contributions

The work presented in this paper has two principal aims. First, we analyze the impact of reduced precision and arithmetic complexity on the algorithm performance and power dissipation in the DS-CDMA mobile RAKE receiver. Next, we explore the architectural design-space for reducing

the on-line power dissipation. Starting with a conventional implementation of the RAKE receiver, we demonstrate design methodologies for achieving power reduction at the algorithm level and the architectural level. This “proof of concept” architecture has been targeted towards a Xilinx Virtex-II FPGA and achieves the targeted data rate of 384 kbps. The resulting power-performance profiles have been obtained after passing synthesized complex receiver data simulating an urban 3 path fading channel through the targeted architectures.

- **Algorithm level:** We show that reduction of sampling rate of the input complex multi-path receiver data to the DS-CDMA RAKE correlator during de-spreading results in favorable trade-offs in power consumption versus the corresponding receiver performance. Significant power savings are achieved through reduction in arithmetic complexity by decreasing the number of arithmetic operations during the RAKE correlation per symbol demodulation. For a 16 bit data-path, we have observed a 24.65% reduction in dynamic power dissipation in the reduced complexity RAKE receiver compared to the reference RAKE receiver implementation, with an acceptable performance loss of less than 2 dB.
- **Architectural level:** Starting with a 16 bit data-path, and reducing precision down to 10 bits, we study the variation in the RAKE receiver performance with decreasing fixed-point precision. Word-length reduction alone results in power reduction of up to 25.6% in the original reference RAKE receiver architecture, and 16.96% further in the reduced complexity RAKE receiver architecture mentioned above.

2 System Description

We consider a K user DS-CDMA downlink system employing Binary Phase Shift Keying (BPSK) symbol modulation during transmission. The k^{th} user's information sequence $b_k \in \{-1, 1\}$ is multiplied by a N chip pseudonoise (PN) sequence whose bit duration equals $T_{bit} = NT_{chip}$. For purposes of estimating the complex channel coefficients [4], a common code-multiplexed pilot signal is broadcast by the base station to all mobile users. The sampled complex receiver data $r(n)$ at the DS-CDMA mobile receiver can be written in vector-matrix notation [3, 6] as $\mathbf{r}_i = \mathbf{S}\mathbf{H}_i\mathbf{A}\mathbf{b}_i + \mathbf{w}_i$ where

- $\mathbf{r}_i$ is the received sampled data (S samples/chip) corresponding to the i^{th} information symbol represented by

$$\mathbf{r}_i = [r(iNST_s) \quad r((iNS + 1)T_s) \quad \cdots \quad r([(i + 2)NS - 1]T_s)]^T \in \mathbb{C}^{2NS \times 1}$$

- $\mathbf{S}$ describes the signature matrix for all K active users and the pilot channel given by

$$\mathbf{S} = [\mathbf{s}_{1,1}, \dots, \mathbf{s}_{1,P}, \dots, \mathbf{s}_{K,1}, \dots, \mathbf{s}_{K,P}, \mathbf{s}_{pilot,1}, \dots, \mathbf{s}_{pilot,P}] \in \mathbb{R}^{2NS \times (K+1)P}$$

Each of the columns $\mathbf{s}_{k,p}$, $1 \leq k \leq K + 1$, $1 \leq p \leq P$ represents the appropriately delayed (by $\lceil \frac{NST_p}{T_b} \rceil$ samples) signature waveform of the k^{th} user and p^{th} multi-path. Therefore,

$$\mathbf{s}_{k,p} = \left[\mathbf{0}_{1 \times \lceil \frac{NST_p}{T_b} \rceil} \quad \mathbf{s}_k^T \quad \mathbf{0}_{1 \times (NS - \lceil \frac{NST_p}{T_b} \rceil)} \right]^T \in \mathbb{R}^{2NS \times 1}$$

and

$$\mathbf{s}_k = [s_k(T_s) \quad s_k(2T_s) \quad \cdots \quad s_k(NST_s)]^T \in \mathbb{R}^{NS \times 1}$$

where $s_k(t)$ represents the k^{th} user's continuous-time spreading waveform given by the convolution of the user's spreading sequence $\{c_k(n)\}$ and the transmitted chip-waveform $g_T(t)$.

- $\mathbf{H}_i$ denotes the complex channel impulse response coefficient matrix for the i^{th} information symbol given by

$$\mathbf{H}_i = \begin{bmatrix} \mathbf{h}_i & 0 & \dots & 0 \\ 0 & \mathbf{h}_i & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & \mathbf{h}_i \end{bmatrix} \in \mathbb{C}^{(K+1)P \times (K+1)}$$

and

$$\mathbf{h}_i = [h_{i,1} \ h_{i,2} \ \dots \ h_{i,P}]^T \in \mathbb{C}^{P \times 1}$$

- $\mathbf{A}$ is the user/pilot amplitude matrix given by $\text{diag}\{A_1, A_2, \dots, A_K, A_{pilot}\} \in \mathbb{R}^{(K+1) \times (K+1)}$
- $\mathbf{b}_i$ is the symbol vector for all K users and pilot corresponding to the i^{th} transmission given by

$$\mathbf{b}_i = [b_1 \ b_2 \ \dots \ b_K \ 1]^T \in \mathbb{R}^{(K+1) \times 1}$$

2.1 DS-CDMA RAKE receiver

The DS-CDMA RAKE receiver attempts to collect the signal energy from all the received signal paths that fall within the delay line and carry the same information [9]. Assuming that user 1 is the user of interest, define the signature matrix,

$$\mathbf{S}_1 = [\mathbf{s}_{1,1} \ \mathbf{s}_{1,2} \ \dots \ \mathbf{s}_{1,p}] \in \mathbb{R}^{2NS \times P}$$

the RAKE receiver computes the decision statistic given by:

$$\begin{aligned} \hat{b}_{1,i} &= \text{sgn}(\mathbf{S}_1 \hat{\mathbf{h}}_i A_1)^H \mathbf{r}_i \\ &= \text{sgn}(\mathbf{S}_1 \hat{\mathbf{h}}_i A_1)^H (\mathbf{S} \mathbf{H}_i \mathbf{A} \mathbf{b}_i + \mathbf{w}_i) \end{aligned} \quad (1)$$

where $\hat{\mathbf{h}}_i \in \mathbb{C}^{P \times 1}$ is the complex channel coefficient estimate obtained from the output of a channel estimator. An all-ones pilot symbol sequence (assumed to be known at the mobile receiver) is used for the purpose of channel estimation. Define

$$\mathbf{S}_{pilot} = [\mathbf{s}_{pilot,1} \ \mathbf{s}_{pilot,2} \ \dots \ \mathbf{s}_{pilot,p}] \in \mathbb{R}^{2NS \times P}$$

as the pilot code signature matrix. Then, the channel estimate $\hat{\mathbf{h}}_i$ is given by the expression $\hat{\mathbf{h}}_i = \sum_{i=n-L+1}^n b_{1,i}^* \mathbf{S}_{pilot}^H \mathbf{r}_i$ where L is the length of the averaging filter.

3 Power-efficient DS-CDMA RAKE receiver architectures

The dynamic power consumption P_{dyn} at any node in a CMOS-based design is a function of the node capacitance C , the switching activity α of the node [defined as the average number of node transitions per clock cycle], the clocking frequency f_{clock} , and the supply-voltage V_{cc} employed in the design, given by $P_{dyn} = \frac{1}{2} \alpha C V_{cc}^2 f_{clock}$. Since P_{dyn} is quadratically related to V_{cc} , voltage reduction yields the biggest savings in power consumption. In addition, optimizations such as reduced algorithmic complexity, re-ordering of arithmetic expressions, word-length reduction can markedly reduce the overall capacitance and node switching activity in the design, thereby reducing the power-dissipation (detailed description is provided in [2, 10]).

Table 1. Arithmetic complexity per symbol detection in the Reference and Reduced Complexity DS-CDMA RAKE receivers employing BPSK signaling.

Operation	Multiplications	Additions
$\mathbf{S}_1^H \mathbf{r}_i \in \mathbb{C}^{P \times 1}$	$4NP/2NP$	$2P(2N - 1)/2P(N - 1)$
$\mathbf{S}_{pilot}^H \mathbf{r}_i \in \mathbb{C}^{P \times 1}$	$4NP$	$2P(2N - 1)$
$\hat{\mathbf{h}}_i = \frac{1}{L} \sum_{k=i-L+1}^i b_k^* \mathbf{S}_{pilot}^H \mathbf{r}_k \in \mathbb{C}^{P \times 1}$	-	$2P(L - 1)$
$\text{Re}(\hat{\mathbf{h}}_i^H \mathbf{S}_1^H \mathbf{r}_i) \in \mathbb{R}^{1 \times 1}$	$2P$	$2P - 1$
RAKE receiver (2 samples/chip)	$(16NP + 2LP - 2P - 1)$ flops	
RAKE receiver (1 sample/chip)	$(12NP + 2LP - 2P - 1)$ flops	

3.1 Reduction in arithmetic complexity

The computationally most intensive operation involved in the RAKE receiver is the correlation operation where the sampled complex multi-path receiver data is correlated with the spreading waveform vector for the user and pilot channels. For the p^{th} finger, the correlation output $X_{cor}^p(i)$ corresponding to the i^{th} signaling interval can be represented by,

$$X_{cor}^p(i) = \int_{iT+\tau_p}^{(i+1)T+\tau_p} r(t) s_1(t - iT - \tau_p) dt \quad (2)$$

where $s_1(t) = \sum_{n=0}^{N-1} c_k(n) g_T(t - nT_c) = (\sum_{n=0}^{N-1} c_k(n) \delta(t - nT_c)) \otimes g_T(t)$. When implementing the correlation operation as a digital matched filter, the complexity of the correlation operation is governed by the length of the signature waveform vector N_{corr} and the number of active fingers P . The signature waveform vector $\mathbf{s}_{1,p}$ is represented by the discrete-time convolution of the length N spreading sequence $\{c_1(n)\}$ and the square root raised cosine filter (pulse-shaping) with impulse response $\{g_T(n)\}$. The length of the pulse-shaping filter equals $M = 2DS + 1$ taps (being linear phase) where D is the group delay of the filter and S is the upsampling rate at the filter input. The length of the convolution output is given by $N_{conv} = M + NS - 1$ samples. Assuming values of $D = 10$ samples, $S = 2$ samples/chip, we obtain $M = 41$, $N_{conv} = 2N + 40$ samples, hence the overall correlator length is specified by $N_{corr} = N_{conv}$. For typical values such as a spreading code of length $N = 32$, $P = 3$ path channel, $L = 16$ tap channel estimator, the arithmetic complexity of the RAKE receiver with ideal correlation equals $16NP + 318P + 2LP - 1 = 2585$ flops/symbol. We explore two schemes for reducing the correlator length as a means for achieving reduction in arithmetic complexity (Table 1).

- **Sampling at 2 samples/chip:** The starting and ending $DS = 20$ samples of the spreading waveform at the convolution output occur due to the group delay of the filter $g_T(n)$. By discarding these $2DS = 40$ samples and retaining the steady state response, the correlator length reduces to $N_{corr} = N_{conv} - 40 = 2N$ samples/symbol, which translates into savings in arithmetic complexity. Thus the number of correlation operations involved in the pilot correlators (for channel estimation) and rake correlators (for despreading and detection) are reduced by $320P = 960$ flops/symbol to 1625 flops/symbol. In the results, the performance of the resulting receiver (with truncated correlation waveform) is shown to be almost identical with that obtained with perfect correlation. We call this receiver as the *reference RAKE receiver*.

Table 2. Fixed-point precision requirements for the RAKE receiver.

Detector Variable	Description	Integer bits
$\mathbf{r}_i \in \mathbb{C}^{2NS \times 1}$	Complex receiver input data	1
$\mathbf{S}_1 \in \mathbb{R}^{2NS \times P}$	User signature matrix	1
$\mathbf{S}_{pilot} \in \mathbb{R}^{2NS \times P}$	Pilot signature matrix	1
$\mathbf{S}_1^H \mathbf{r}_i \in \mathbb{C}^{P \times 1}$	Soft Rake Correlator Output	3
$\mathbf{S}_{pilot}^H \mathbf{r}_i \in \mathbb{C}^{P \times 1}$	Soft Pilot Correlator Output	3
$\sum_{k=i-L+1}^i b_{1,k}^* \mathbf{S}_{pilot}^H \mathbf{r}_k \in \mathbb{C}^{P \times 1}$	Moving Average Accumulator	5
$\hat{\mathbf{h}}_i = E[b_{1,i}^* \mathbf{S}_{pilot}^H \mathbf{r}_i] \in \mathbb{C}^{P \times 1}$	Channel coefficient Estimate	3
$(\mathbf{S}_1 \hat{\mathbf{h}}_i \mathbf{A}_1)^H \mathbf{r}_i \in \mathbb{C}^{1 \times 1}$	Maximal Ratio Combiner output	6

- **Sampling at 1 sample/chip:** To achieve a reduction in the arithmetic complexity, we reduce the sampling rate for the despreading operation in the RAKE correlators to 1 sample/chip, and investigate the resulting complexity vs. performance trade-offs. This halves the length of the correlator for the RAKE despreading operation to $N_{corr} = N$ samples/symbol and a corresponding reduction in the overall operation count by $4NP = 384$ flops/symbol to 1241 flops/symbol. As the performance of detection is heavily influenced by the accuracy of channel estimates, the pilot channel correlation is still performed at 2 samples/chip. The complexity reduction comes at the tradeoff of reduced correlator output energy owing to the halved correlation length. The results demonstrate a significant power reduction with acceptable detection performance due to this optimization. We call this receiver as the *reduced complexity RAKE receiver*.

3.2 Reduction in fixed-point Precision

All the DS-CDMA architectures presented in this paper are based on a fixed-point implementation. A quantization analysis tool developed at the University of Texas, Dallas [7] was used for determining the dynamic range and precision requirements of the RAKE receiver. Table 2 shows the fixed-point integer requirements of the individual RAKE receiver variables after quantization analysis. From the obtained fixed-point formats, extensive simulations were carried out using MATLAB/C with C++ classes in SystemC providing the fixed-point arithmetic support. A minimum word-length of 10 bits was required for the RAKE receiver to achieve acceptable performance (within 1 dB) of the equivalent floating point version of the algorithm.

3.3 Architecture description

Two distinct architectures incorporating the aforementioned power saving techniques were implemented on a Virtex-II FPGA.

- **Reference architecture:** Figure 2 shows the reference architecture of the RAKE receiver. This implementation employs a uniform input sampling rate of 2 samples/chip for both the PILOT and RAKE correlator matched filtering operations. The external clock is passed through a delay-locked loop to derive the global clock buffer CLK running at the input sample frequency of $f_{samp} = 24.576$ MHz.

Figure 2. Architecture of the reference DS-CDMA downlink RAKE receiver.

- Reduced Complexity architecture:** To explore the effects of reduced arithmetic complexity on the resulting power consumption of the RAKE receiver, the wide-band signal was input at the rate of 2 samples/chip to the PILOT correlator and 1 sample/chip to the RAKE correlator. Figure 3 shows the architecture of the resulting reduced complexity RAKE receiver with two separate clocking domains namely CLK (shown by the solid box) and CLK_{DV} (shown by the dashed box) running at $f_{samp} = 24.576$ MHz and $\frac{f_{samp}}{2} = 12.288$ MHz respectively. While the global clock buffer distribution CLK was used to clock the PILOT matched filtering operation, the second clock buffer CLK_{DV} was used to clock the RAKE matched filtering, channel estimation and Maximal Ratio Combining blocks. The presence of two independent clocking domains required the use of additional synchronizing logic to transfer signals (such as the pilot soft matched filter output) from the CLK domain to CLK_{DV} domain.

4 Results

For studying the impact of precision reduction on the resulting algorithm performance, the mobile receivers were simulated based on 10,12,14,16 bit fixed-point word-length and compared with a floating point implementation. For each word-length format, the average received $SNR = 10 \log_{10}(\frac{E_b}{N_0})$ was varied to study the effect on the bit-error rate performance of the algorithm. In the computer simulations, 5 equal power users employing length 32 extended Gold sequences were considered. The scenario in consideration was a 5 user, 3 path correlated Rayleigh fading channel based on the Jakes mobility model. For each data-point, 40 random test cases of 5000 transmitted bits were tested. The multi-path delays were fixed for each simulation and varied from one simulation to the next. All the users were assigned unit transmit amplitudes. An additional code-multiplexed pilot channel with a 3 dB higher power was employed for channel estimation at the mobile receiver. The over-sampling rate at the transmitter and receiver front end was chosen to be 2 samples/chip in order to account for fractional multi-path delays. The A/D converter at the

Figure 3. Architecture of the DS-CDMA downlink RAKE receiver with reduced complexity.

receiver front end was chosen to have an 8 bit width (*S8Q7* format). We consider the performance of the following DS-CDMA RAKE receivers:

- Reference RAKE receiver performing truncated correlation sampled at 2 samples/chip (Complexity= $16NP - 2LP - 2P - 1$ operations/symbol).
- Reduced arithmetic complexity RAKE receiver performing truncated correlation sampled at 1 sample/chip for detection and 2 samples/chip for channel estimation (Complexity= $12NP - 2LP - 2P - 1$ operations/symbol).

The performance of these receivers were compared against a DS-CDMA RAKE receiver employing perfect correlation (highest complexity of $16NP + 318P + 2LP - 1$ operations/symbol).

4.1 Multi-user, Multi-path fading channel

Figure 4 shows the performance of the reference DS-CDMA RAKE receiver for the above scenario. We notice that the receiver performance in fixed-point is close to the ideal floating point performance, with negligible performance degradation for the 10 bit precision (less than 1 dB loss) upto an SNR of 10 dB. Figure 5 shows the performance of the reduced complexity DS-CDMA RAKE receiver. The reduction in complexity for reducing the dynamic power consumption, causes a performance degradation of 2 dB compared to the ideal DS-CDMA RAKE receiver employing ideal correlation (shown by the dashed line in black), owing to the reduced energy at the output of the RAKE correlator. We note that the receiver performance in fixed-point is almost identical with the floating-point performance up to a 10 bit precision.

Figure 4. Error Probability vs. Average SNR for Reference DS-CDMA RAKE receiver (multi-user).

Figure 5. Error Probability vs. Average SNR for Reduced Complexity DS-CDMA RAKE receiver (multi-user).

4.2 Results of FPGA implementation: Timing simulation

The RAKE receiver architectures were targeted for a 2 million gate Virtex-II (XC2V2000 series) FPGA. Synthesized complex receiver data for an urban 3 path Rayleigh multi-path channel was passed through each receiver implementation, and symbol detection was carried out. For finding the dynamic power consumption in the design, the synthesized receiver data was run through the receiver. An external clock running at 50 MHz was produced to clock the receiver. The analysis was carried out following the synthesis, translation, mapping, netlist extraction, and the post-placement and routing phase. Extensive timing simulations were carried out in the Modelsim simulator to model true-device behavior. All internal node transitions occurring during the course of the simulations were dumped into a “.vcd” (Value-Change-Dump) file format. The .vcd files were then analyzed by the power analysis tool XPower provided by Xilinx. The dynamic power consumption was obtained after calculating the difference of the overall design power consumption and the quiescent power (225 mW) of the FPGA.

In Table 3, the results of implementation of the reference and reduced complexity architectures have been reported. The area shown in the table is represented in FPGA slices as well as the percentage occupancy in the FPGA, with the available area being 10752 slices in a Virtex-II FPGA. Considering *only* the effect of reduced precision, the reference architecture family shows a power reduction of 25.6% for the 10 bit data-path compared to the 16 bit data-path. Within the reduced complexity architecture family, we observe power savings of 16.96% for the 10 bit data-path compared to the 16 bit data-path. These power savings are quite significant considering that the 10 bit data-path achieves almost close to the equivalent floating point performance for both the reference and reduced complexity receivers (performance loss being less than 1 dB).

Next, we consider the additional effect of complexity reduction on the resulting power savings. The 16 bit reduced complexity RAKE receiver achieves a power saving of 24.65% compared to the 16 bit reference RAKE receiver implementation. The combined effect of reduced precision and arithmetic complexity results in 37.4% reduction in dynamic power consumption for the 10 bit RAKE receiver, with a 3 dB degradation in performance (Figure 5). The tradeoff of dynamic baseband power consumption with receiver performance is important for battery operated mobile wireless terminals. In scenarios where there is a strong received signal, then adaptive methods to reduce the dynamic digital baseband processing as proposed in this paper will greatly increase battery life.

5 Conclusion

We have examined design methodologies and performance trade-offs for reducing the online power dissipation in a DS-CDMA mobile RAKE receiver. At the algorithm level, reduction in arithmetic complexity has been investigated for obtaining savings in the dynamic power dissipation. At the architectural level, precision reduction and activity rate reduction have been exploited for additional savings.

Reduction in precision shows that a 10 bit data-path achieves near floating point performance with minimal performance degradation for the reference RAKE receiver. Power-efficient architectures based on a Xilinx Virtex-II FPGA have been proposed for implementing both the conventional and reduced complexity DS-CDMA RAKE receiver. For a 16 bit data-path, we have observed a

Table 3. FPGA implementation of Reference and Reduced Complexity architectures for the DS-CDMA downlink RAKE receiver.

Type	Bits	Area (Slices)	P_{dyn} (mW)	Savings
Reference	16	3572(33%)	109.5	-
	14	3000(28%)	97.5	10.95%
	12	2341(22%)	93	15.06%
	10	1844(17%)	81.5	25.6%
Reduced Complexity	16	3724(35%)	82.5	24.65%
	14	3134(29%)	73	33.33%
	12	2457(23%)	68.5	37.44%
	10	1942(18%)	68.5	37.44%

24.65% reduction in dynamic power dissipation in the reduced complexity RAKE receiver compared to the reference RAKE receiver implementation, with an performance loss of less than 2 dB. The combined effect of reduced precision and complexity reduction leads to a 37.44% savings in digital baseband power consumption which will extend the operation of mobile wireless terminals.

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